06,13

A weak manifestation of the field effect in metal-dielectric-semiconductor structures with a ferroelectric insulating layer $Ba_xSr_{1-x}TiO_3$

© D.A. Belorusov, E.I. Goldman, G.V. Chucheva ¶

Fryazino Branch, Kotel'nikov Institute of Radio Engineering and Electronics, Russian Academy of Sciences, Fryazino, Moscow oblast, Russia

¶ E-mail: gvc@ms.ire.rssi.ru

Received June 29, 2021
Revised June 29, 2021
Accepted July 3, 2021

High-frequency measurements of the capacitance and conductivity of Ni-$Ba_{0.8}Sr_{0.2}TiO_3$-Pt and Ni-$Ba_{0.8}Sr_{0.2}TiO_3$-Si objects with a ferroelectric thickness of 120 nm in the paraelectric phase were carried out. It is shown that in the entire range of external voltages, the electric field practically does not penetrate Si. The conclusion made earlier about the reasons for the weak manifestation of the field effect is confirmed — the polarization of the ferroelectric layer is almost completely shielded by the charges of electronic traps at the $Ba_{0.8}Sr_{0.2}TiO_3$-Si contact. It is noted that a sharp decrease due to passivation of the activity of surface traps will allow implementing transistors based on metal-BST-Si structures with a working surface channel of non-basic charge carriers and will ensure the construction of high-quality FeRAM non-volatile memory cells.

Keywords: metal-dielectric-semiconductor-structures, metal-dielectric-metal-structures, ferroelectric films of the composition $Ba_{0.8}Sr_{0.2}TiO_3$, high-frequency impedance.

DOI: 10.21883/PSS.2022.13.52316.154

1. Introduction

Ferroelectric films are one of the preferred alternatives to insulating silica layers used in electronic devices [1]. The unique physical properties of ferroelectric materials (specifically, their high permittivity, which can be adjusted by an external electric field) provide an opportunity to fabricate essentially new classes of planar devices for data storage and processing [2]. Solid solutions of barium strontium titanate $Ba_{1-x}Sr_xTiO_3$ (BST) exhibit ferroelectric properties above room temperature, and their dielectric constant also remains fairly high in the paraelectric phase. Although BST films have been studied since the late 20 th century [3,4], no reports regarding transistor structures based on these ferroelectric materials with functional surface conductance channels for minority carriers in nanometer-sized semiconductors have been published to date [5]. The experiments in [6], which involved Ni-BST-Si structures with a ferroelectric $Ba_{0.8}Sr_{0.2}TiO_3$ film with thickness $h = 350$ nm, revealed one possible reason for the weak manifestation of the field effect: an almost complete screening of the ferroelectric layer polarization by the charges of electron traps in the interface layer at the contact with silicon. This is an important result, since the methods for trap passivation in the interface layer, which were tested well in the silicon planar process, offer prospects for creating a surface conductance channel for minority carriers in a semiconductor and thus make the projects of fabrication of non-volatile FeRAM cells based on structures with BST practicable. In order to advance the studies in this direction, one needs to ascertain that the conclusions made in [6] generalize to structures with different thicknesses of ferroelectric films deposited on *n*- and *p*-type substrates. The present study is thus focused on verifying the results presented in [6] by examining Ni-BST-Si and Ni-BST-Pt samples with a thinner ($h = 120$ nm) ferroelectric layer.

2. High-frequency impedance of Ni-$Ba_{0.8}Sr_{0.2}TiO_3$-Si and Ni-$Ba_{0.8}Sr_{0.2}TiO_3$-Pt structures

A one-dimensional model of the high-frequency (HF) impedance of metal–ferroelectric–semiconductor structures with a buffer layer at the contact with the substrate was developed in [6]. This model provides an opportunity to determine the charge density in the buffer layer between BST and Si and the band bending in the semiconductor (as a function of the external voltage) by analyzing the experimental characteristics of such structures and metal–ferroelectric–metal samples. Technically, this model is applicable only in the paraelectric phase of the insulating layer. Therefore, the HF characteristics need to be measured at temperatures well above room temperature.

Ni-BST-Pt and Ni-BST-Si structures with area $S = 2.7 \cdot 10^{-4}$ cm^2 were used in the experiments. The same *n*-type silicon used in [6], $N_d = 2.4 \cdot 10^{14}$ cm^{-3} with a platinum sublayer or natural oxide on the wafer surface, served as substrates. A ferroelectric film with thickness $h = 120$ nm was deposited by HF sputtering of a polycrystalline target in oxygen atmosphere in a Plazma-50SE (Russia) setup. The design of this setup and the film deposition technique were discussed in greater detail in [7,8]. Impedance measurements were carried out

in the paraelectric phase in the 110–130°C temperature range at the same frequency (1 MHz) as in [6] using an Agilent E4980A precision LCR meter, a portable computer with updated software, and a specialized camera fitted with a warm table with thermal stabilization. A detailed description of the experimental setup was given in [9].

The results of experiments for a measurement temperature of 121°C are shown in Figs. 1 and 2.

The curves for other temperatures are similar in shape to the presented ones. As in [6], the following inequalities are true: $(G/\omega C) \propto (1/100) \ll 1$, $(C_{SE}/C) \propto 10 \div 100 \gg 1$, where C and G are the capacitance and the conductivity of Ni-BST-Si structures, C_{SE} is the capacitance of the Ni-BST-Pt sample, and ω is the angular frequency of impedance measurements. It follows from the formula for the HF impedance [6, formula (5)] that

$$1 \gg \frac{C}{\omega C} > \left\{ \left[1 - \frac{\left(C + \frac{G^2}{\omega^2 C}\right)}{C_s} \right] \times \left[\frac{\left(C + \frac{G^2}{\omega^2 C}\right)}{C_{SE}} + \frac{\left(C + \frac{G^2}{\omega^2 C}\right)}{C_s} - 1 \right] \right\}^{1/2}. \quad (1)$$

Here, C_s is the capacitance of the charged region of silicon adjacent to BST. Therefore, just as in [6], the following remains true for our samples in the entire range of applied voltages:

$$C \cong C_s. \quad (2)$$

Thus, tabularizing the dependence of C_s on band bending in the semiconductor V_s in accordance with the expressions for classical statistics [10]

$$C_s = \frac{C_{sfb}}{2^{(1/2)}} \frac{|1 - e^{-\nu_s}|}{(e^{-\nu_s} + \nu_s - 1)^{(1/2)}}, \quad \nu_s = -\frac{qV_s}{T}, \quad (3)$$

one may use the chain of interrelations $V_g \Rightarrow C = C_s \Rightarrow \nu_s \Rightarrow V_s$ to plot the dependence of the band bending on external voltage V_g. Here, C_{sfb} is the semiconductor capacitance in the flat-band state ($V_s = 0$); $\nu_s = -\frac{qV_s}{T}$ is the dimensionless band bending in the semiconductor, $\nu_s > 0$ at depletion of the silicon surface; q is the elementary charge; T is absolute temperature in energy units. The semiconductor capacitance in the flat-band state was calculated in [6]: $C_{sfb} = 9.17$ pF. The obtained dependence of V_s on V_g is presented in Fig. 3.

It follows from the $V_s(V_g)$ plot that the band bending in silicon is many times smaller in magnitude than the applied voltage. The variation of ν_s with V_g in depletion is restricted more severely than in enhancement, $-5 < \nu_s < 2$. The low sensitivity of the band bending in the semiconductor to the variation of V_g gives rise to plateaus in the field dependences of the HF capacitance and the conductivity of the structure. The lower plateau, where the $V_s \approx$ const condition is fulfilled more exactly, is characterized by a weaker voltage dependence of C and G than the upper one.

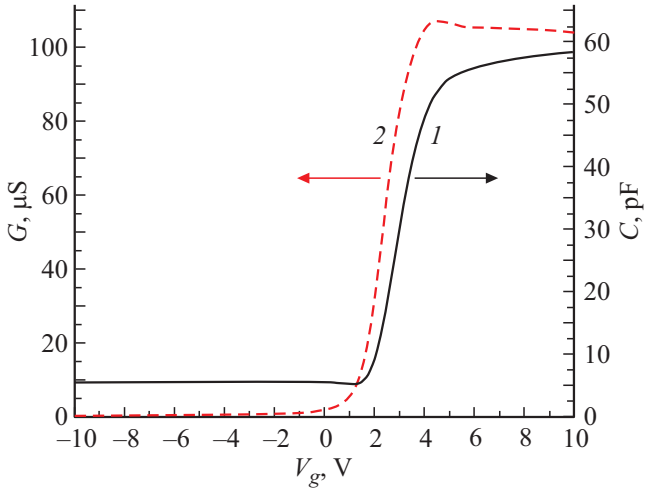

Figure 1. High-frequency field characteristics of the Ni-$Ba_{0.8}Sr_{0.2}TiO_3$-Si structure with a ferroelectric layer thickness of 120 nm measured at $T = 121$°C. Curves *1* and *2* correspond to the capacitance and the conductivity, respectively.

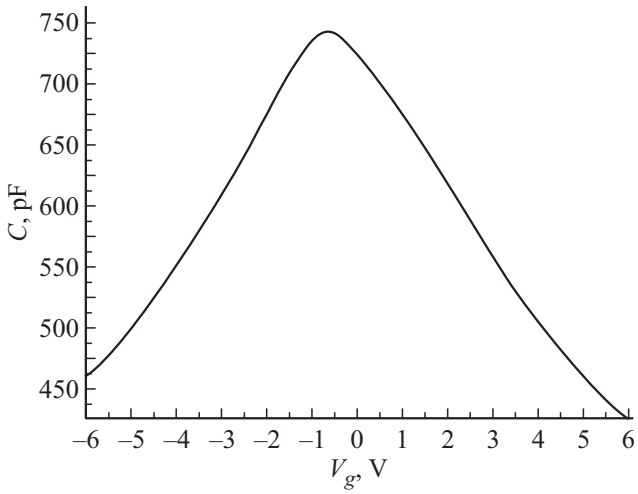

Figure 2. High-frequency capacitance-voltage curve of the Ni-$Ba_{0.8}Sr_{0.2}TiO_3$-Pt structure with a ferroelectric layer thickness of 120 nm measured at $T = 121$°C.

Thus, the findings presented in [6] were reproduced accurately in experiments with samples with another thickness of the ferroelectric material: the weak manifestation of the field effect in metal–dielectric–semiconductor structures with a ferroelectric insulating $Ba_{1-x}Sr_xTiO_3$ layer is attributable to the charge exchange with surface electron traps in the interface layer. It is these localized states that establish an almost complete screening of polarization of the ferroelectric layer in the metal–BST–Si structure. Judging by the external voltage swing (10 V) and using the estimate of the trap charge ($C_{SE}V_g$), we find that the density of traps should be no lower than 10^{14} cm^{-2}. Here, we can make only the most general assumptions regarding the nature of traps. The buffer layer between the ferroelectric material and Si

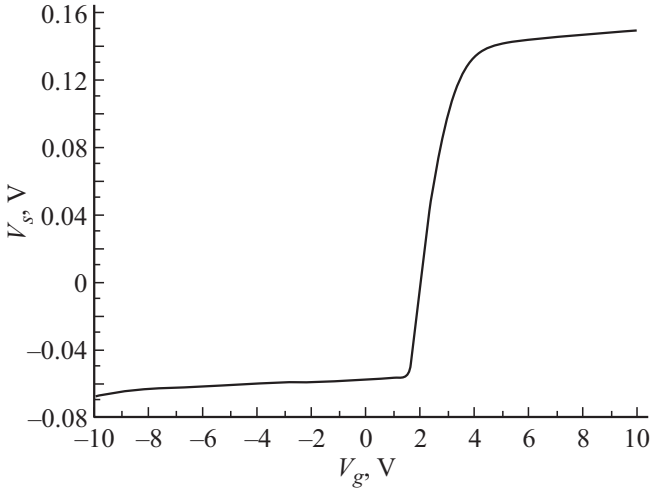

Figure 3. Dependence of band bending V_s in silicon on external voltage V_g in the Ni-$Ba_{0.8}Sr_{0.2}TiO_3$-Si structure.

is made primarily of silica; the surface levels on Si-SiO_2 interfaces correspond to the paramagnetic states of Si atoms with an unpaired electron coupled with three atoms in the bulk of the semiconductor, $\equiv Si_3Si\bullet$ (so-called P_b centers or dangling bonds [11]). In theory, the density of these dangling bonds is $8 \cdot 10^{14}\,cm^{-2}$, and they undergo charge exchange under both depletion and enhancement of the semiconductor [11]. Therefore, P_b centers are well-suited for the role of electron traps in metal−BST−Si samples.

3. Conclusion

Let us reiterate an important point from [6]: the objects with a ferroelectric insulating layer studied in our experiments and metal−SiO_2−Si structures tested in the 1960s and 1970s, when active traps at the contact between silicon and silica hindered the fabrication of high-quality transistors with a conductance channel for minority carriers, are somewhat similar. Industrial engineers solved the mentioned problem by passivating the dangling bonds with hydrogen. Therefore, it is natural to make use of the experience accumulated in the silicon planar technology and suppress the activity of electron traps in the interface layer in the process of fabrication of metal−BST−Si structures. This should provide an opportunity to fabricate metal−BST−Si transistors with a functional surface conductance channel for minority carriers and engineer high-quality nonvolatile FeRAM cells.

Funding

This study was carried out within the framework of a state assignment and partially supported by the Russian Foundation for Basic Research (projects Nos. 18-29-11029, 19-07-00271, and 19-29-03042).

Conflict of interest

The authors declare that they have no conflict of interest.

References

[1] V.R. Mudinepalli, L. Feng, W.-C. Lin, B.S. Murty. J. Adv. Ceram. **4**, 46 (2015).
[2] K.A. Vorotilov, V.M. Mukhortov, A.S. Sigov, Integrirovannye segnetoelektricheskie ustroystva, Ed. A.S. Sigov (Energoatomizdat, M., 2011), 175 pp. (in Russian).
[3] H. Kawano, K. Morii, Y. Nakayama. J. Appl. Phys. **73**, *10*, 5141 (1993).
[4] S. Ezhilvalavan, T.Y. Tseung. Rev. Mater. Chem. Phys. **65**, 227 (2000).
[5] J.Y. Park, K. Yang, D.H. Lee, S.H. Kim, Y. Lee, P.R. Sekhar Reddy, J.L. Jones, M.H. Park. J. Appl. Phys. **128**, *24*, 240904 1−24 (2020); doi: 10.1063/5.0035542
[6] E.I. Goldman, G.V. Chucheva, D.A. Belorusov. Ceram. Int. https://doi.org/10.1016/j.ceramint.2021.04.129
[7] M.S. Ivanov, M.S. Afanasiev, Phys. Solid State **51**, *7*, 1259 (2009).
[8] D.A. Kiselev, M.S. Afanasiev, S.A. Levashov, G.V. Chucheva, Phys. Solid State **57**, *6*, 1134 (2015).
[9] E.I. Gol'dman, A.G. Zhdan, G.V. Chucheva, Instrum. Exp. Tech. **6**, 110 (1997).
[10] S.M. Sze, Kwok K. Ng. Physics of Semiconductor Devices. Willey Interscience publication (2007).
[11] V.A. Gritsenko. Phys.-Usp. **52**, *9*, 869 (2009).