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NANOELECTRONICS

Ultrathin (3.7 nm) Silicon Oxide Layers with a Low Concentration of Broken Bonds on the Contact with a Semiconductor

D. A. Belorusov[a], E. I. Goldman[a], and G. V. Chucheva[a, *]

[a] *Kotelnikov Institute of Radioengineering and Electronics, Fryazino Branch, Russian Academy of Sciences, Moscow oblast, Fryazino, 141190 Russia*

**e-mail: gvc@ms.ire.rssi.ru*

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Abstract—Results of studies of ultrathin silicon oxide (37 Å)—polysilicon structures as prospects of substrates for objects with ferroelectric insulating layers are presented. It turned out that in structures with SiO_2 obtained by high-temperature oxidation, there are low leakage currents associated with tunneling conduction, and the concentration of localized electronic states is three orders of magnitude lower than in objects with native oxide. These circumstances open prospects of creating ferroelectric FeRAM non-volatile memory cells operating on such silicon oxide.

Keywords: metal—ferroelectric—silicon structures, buffer layer, ultrathin oxide, high-frequency current—voltage characteristics, capacitance—voltage characteristics

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INTRODUCTION

Integrated circuits composed of metal—oxide—semiconductor (MOS) silicon structures form the basis of modern electronics. The transition to nanosized MOS objects has led to the achievement of the minimum allowable thickness of silicon oxide. Therefore, research has been ongoing for several decades on various dielectric materials being developed as an alternative to SiO_2 [1–3]. In the overwhelming majority of cases, silicon wafers serve as substrates for such insulators. Due to the significant mismatch of crystal lattices, when a ferroelectric is deposited on a semiconductor, a so-called buffer layer [3] is formed, which consists mainly of oxides of the contacting materials. It is well known [4] that the surface of Si substrates is always covered with oxide. It can be either natural (native) SiO_2, arising from the oxidation of a semiconductor in the atmosphere, either artificially prepared, or as a result of precipitation, or reaction with oxygen at high temperatures. Naturally, the properties of the oxide, and, consequently, of the buffer layer, are largely determined by the technology of SiO_2 preparation on the surface of the substrate. Dangling Si bonds are always formed at the interface (IF) between silicon and oxide, which play the role of electron traps (ETs) [4]. Theoretically, their concentration can reach 8×10^{14} cm^{-2}, and they are recharged both during depletion and enrichment of the semiconductor [5]. The actual density of dangling bonds depends on the oxide preparation technology and in some cases decreases to units of 10^{10} cm^{-2} [4]. The conductivity of the oxide is associated with electron hopping over electronic states, including dangling bonds of silicon in the bulk of SiO_2, and largely depends on the packing density of the insulator and the processes of electron trap passivation [4]. High-quality oxides obtained by high-temperature oxidation are characterized by a decrease in conductivity up to the transition to tunneling through the SiO_2 layer.

Previously, based on structures with the ferroelectric $Ba_{0.8}Sr_{0.2}TiO_3$ deposited on silicon, it was experimentally shown [6, 7] that ETs recharging in the buffer layer prevents the development of the field effect, its penetration into the semiconductor, thereby preventing the implementation of FeRAM non-volatile memory cells. Since the transition layers between the silicon substrate and the insulator are generally typical for such contacts, no manifestation of the field effect can be observed in other Si-based transistor structures, including those with a non-ferroelectric dielectric layer other than SiO_2. Therefore, for the development of ferroelectric and other ferroelectric devices compatible with planar technology, which differ from Si—SiO_2 transistor structures, it is necessary to use substrates with high-quality silicon oxide on the surface, with a small contribution of non-tunnel leakage currents and with a minimum content of dangling bonds on the Si—SiO_2 IF. At the same time, the achievable limits of the minimum concentrations of dangling bonds remains an important issue. And, although the history of the study of MOS structures with ultrafine SiO_2 has been going on for several decades, it is diffi-

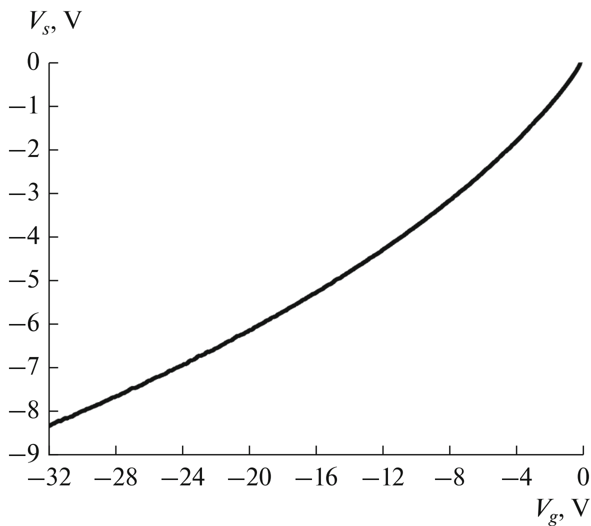

Fig. 1. Depletion band bending V_s in a semiconductor depending on field voltage V_g.

cult to draw quantitative conclusions from disparate data obtained under different external conditions on samples with oxide formed by various technologies. The main problem is that the measurements of current and high-frequency capacitances refer to the same state of the sample, i.e., almost completed at the same time. Experimental studies are needed from which it will become clear what properties of buffer layers on a contact other than a SiO_2 insulator with silicon are achievable in the light of the manifestation of a Si–SiO_2 IF. Such experiments should be carried out in a special non-stationary mode [8], which ensures the invariance of the state of the sample during each measurement, at the highest quality[1] MOS structures with ultrafine SiO_2 (thickness up to 5 nm), grown by high-temperature oxidation. This study is devoted to these experiments and its novelty is due to the solution of problems that have arisen recently, specific for buffer layers on contacts other than SiO_2 insulators with silicon, and the application of new methodological approaches.

1. EXPERIMENTAL RESULTS

As samples, we used Si-MOS structures with an Al–n^+-Si:P (donor concentration in polysilicon of $N_d^+ \sim 10^{20}$ cm^{-3}, field electrode area S = 1.6×10^{-3} cm^2) isolated from a (100) n-Si substrate layer obtained by high-temperature oxidation of SiO_2 with an optical thickness of $h = 3.7$ nm. These objects belong to the group of structures [8, 9] in which there is practically no response to a field effect of the damage type, i.e., with an increase in the duration of exposure at field voltages of different polarity, up to the transition to a soft breakdown state, neither the conductivity through the oxide nor the distribution of the built-in charge practically change in the objects. The experiments were carried out at room temperature on an automated setup [9] and included measurements of current–voltage (CVCs) and high-frequency capacitance–voltage characteristics of objects at frequencies of 1 (C_1) and 0.5 (C_2) MHz using an Agilent E4980A precision LCR meter. The experiments were carried out in a non-stationary special mode [8], when the values of high-frequency capacitances and current during their fixation correspond to practically the same state of the sample. Experience scheme: for each measurement point from the position, field voltage $V_g = 0$ was the specified bias applied to sample V_g; after the end of RC processes (less than 0.3 s), current I through the oxide was fixed, then within 5 s of capacity C_1 and C_2. After that, the applied voltage dropped to zero, and the structure was held for 5 s. The total duration of measurements of the current and capacitances at the same value of the voltage on the field electrode is significantly less than the characteristic time of the transient process associated with the recharging of localized electronic states on the Si–SiO_2 IF (more than 15 s). This procedure makes it possible to minimize the duration of the sample's stay in pre-breakdown conditions during measurements. The capacitance–voltage characteristic data corresponding to two high frequencies make it possible to carry out certification of the sample [10, 11], to determine the concentration of donors at the Si–SiO_2 IF, the resistance of the semiconductor substrate and plot the dependences on the field voltage of the following quantities: band bending V_s in the semiconductor, external voltage drop V_i across the insulating layer and, generally speaking, expressed in cm^{-2} the total density of the built-in charge, charge p_{sq} of the boundary states and holes on the IF [12]. The results of such processing of the measured current values as a function of the voltage on the oxide and the relationship of this voltage, as well as the bending of the bands in a semiconductor with an external bias, are shown in Figs. 1–3.

Note that for samples with ultrafine SiO_2 often building an experimental dependence $p_{sq}(V_g)$ from the data of high-frequency measurements is impossible due to the inaccuracy in determining capacity C_i of the oxide. The fact is that for such objects it becomes important to take into account the transition layers at the contacts with the semiconductor and the gate (they make up 35% or more of the volume). In these layers, the permittivity decreases with the coordinate from the values for silicon to the value for oxide. Therefore, the values of the SiO_2 capacitance obtained by calculation without taking into account the transi-

[1] Those with conductivity associated with direct tunneling and a minimum amount of ETs in the bulk of the oxide film and IF with silicon.

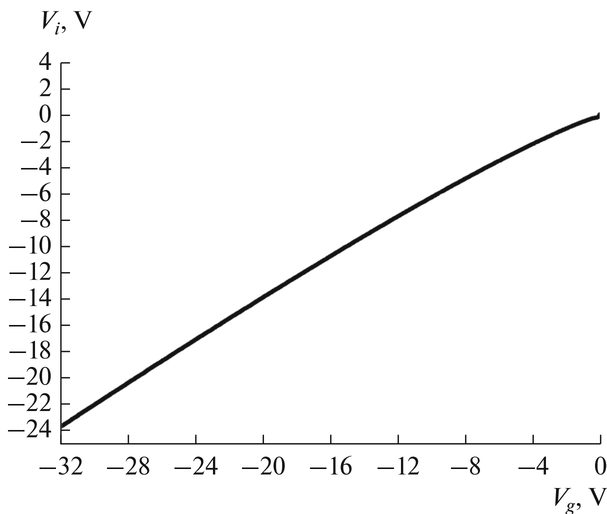

Fig. 2. Oxide voltage drop V_i depending on external offset V_g.

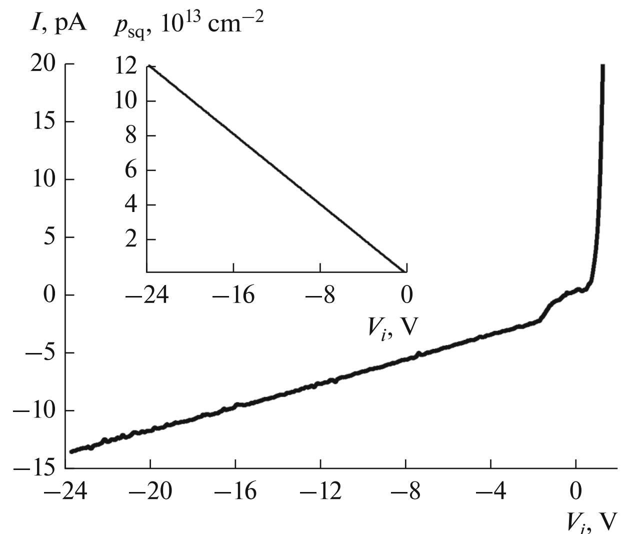

Fig. 3. The dependence of the current I through the oxide against voltage drop V_i across the insulating layer. The inset shows a graph of the total concentration of holes and rechargeable traps $p_{sq}(V_i)$.

tion layers different from the real ones. In practice, the value of C_i is defined as the maximum value of the capacitance of the MOS structure on a plateau in a state of deep silicon enrichment. But in this region, in real cases, when the semiconductor surface is deeply degenerated only under breakdown or pre-breakdown conditions, the capacitances of the insulating gap and silicon can be of the same order. Therefore, the value determined from the maximum value of C_i on the plateau will be much less than the real one. Because dependence $p_{sq}(V_g)$ is calculated as the difference between two terms, one of which is directly proportional to the capacity of the oxide, then the error in the value of C_i seriously affects the result: an almost straight line appears on experimental graph $p_{sq}(V_i)$ associated with this error. It is this case that was realized in our samples, see the inset to Fig. 3.

In the mode of our measurements, the ETs on the Si–SiO_2 IFs practically do not have time to recharge. Accordingly, it is impossible to determine their concentration from these data. The detected current contains contributions from four processes: tunneling of electrons from the gate polysilicon to the semiconductor and vice versa, rearrangement of the distribution of free electrons in silicon at the contact with the oxide, recharging of dangling bonds on the IF, and generation of minority charge carriers. In this case, the main component in the leakage current is the tunnel component. Therefore, only relaxation experiments can be used to determine the ET concentration, when changes in the measured values are due only to the recharging of dangling bonds. Moreover, it is convenient to take a voltage step that enriches silicon, since in this case minor charge carriers do not arise. The time dependences of the current and capacitance (1 MHz) of the MOS structure after applying a bias of 1 V to the sample are shown in Fig. 4.

2. RESULTS AND DISCUSSION

Figures 1 and 2 confirm the significant influence of the nonstationarity of the conditions under which the measurements were made. In equilibrium, in a state of deep inversion of the silicon surface, screening of the external field by minority charge carriers limits the band bending in the semiconductor to a value of about 1 V, and the rest of the external voltage must fall on SiO_2. In our case, due to the delay in the effects of hole generation and recharging of ETs on the Si–SiO_2 IF the external bias is divided between the semiconductor and the oxide almost inversely with the permittivities. Achieved field values of 6×10^7 V/cm in the insulating layer testify to the high quality of silicon oxide in these samples. The magnitude of band bending in silicon (several volts) is sufficient with a margin to open the surface channel of minority charge carriers. From Fig. 3 it can be seen that at the same modulus voltages on SiO_2 currents in the region of strong depletion of the semiconductor are orders of magnitude smaller than in the case of enrichment of silicon. Such a significant asymmetry of the CVC of an ultrafine oxide is, generally speaking, not typical of MOS objects, but is characteristic of a separate group of undamaged samples [8, 9]. The reasons for this phenomenon were studied in [13], where it was shown that the real potential barrier of the oxide of undamaged MOS structures is thinner than the SiO_2 film and is significantly shifted to contact with the field electrode.

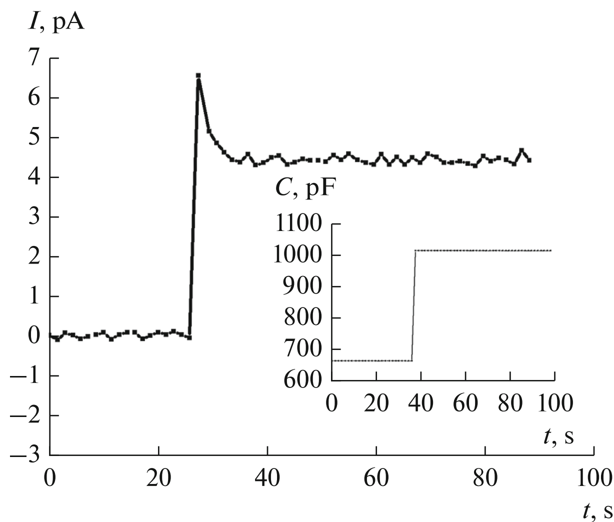

Fig. 4. The transient process in the MOS structure after enrichment voltage step $V_g = +1$ V. The inset shows the time dependence of the capacitance of the structure at a frequency of 1 MHz.

Let us estimate the ET concentration on the Si–SiO_2 IF in our MOS structure. From Fig. 4 it follows that the current drop after relaxation on the step is 2.24 pA. In this case, the capacitance practically does not change in the process of establishing a stationary state (see the inset to Fig. 4). This means that the currents associated with the rearrangement of the charge of free electrons near the semiconductor surface can be neglected. Therefore, during the transient process of 15 s, 1.05×10^8 will be recharged dangling bonds, which corresponds to their concentration of 6.6×10^{10} cm^{-2}. This value is at least 2 orders of magnitude smaller than that obtained from the curve in the inset to Fig. 3 and the ET density values found in the buffer layer on the $Ba_{0.8}Sr_{0.2}TiO_3$–Si contact [6, 7]. Naturally, the simplest processing of the time dependence curve of the ET recharging current cannot replace successive studies of the spectrum and lifetimes of electrons in the states localized in Si–SiO_2 IFs. However, the low ET concentration found gives hope for the prospects for using structures with insulating layers other than SiO_2, based on silicon substrates with high-quality oxide.

CONCLUSIONS

The results show that for metal–insulator structures made of a material other than SiO_2, the use of silicon coated with high-quality oxide can significantly improve the characteristics of buffer layers and, apparently, remove restrictions on the opening of the minority carrier channel, which is necessary for the development of various devices, in particular, for the implementation of FeRAM non-volatile memory cells. Application as substrates of Si coated with SiO_2 obtained by high-temperature oxidation, will certainly reduce leakage currents and stabilize the properties of objects with new insulating layers compared to silicon oxide.

The development of work in the direction of optimizing the quality of substrates for structures with such insulating layers requires relaxation spectroscopy of localized electronic states on a silicon-ultrafine oxide IF. Such spectroscopic studies should be performed on the basis of relaxation measurements of currents in the gate–substrate circuit at low (up to 77 K) temperatures in the mode of maintaining the high-frequency capacitance of the structure constant in time.

CONFLICT OF INTEREST

The authors declare that they have no conflicts of interest.

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