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On the form of high-frequency voltage-capacitance characteristics of metal-insulator-semiconductor structures with a ferroelectric insulating layer $Ba_xSr_{1-x}TiO_3$

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ABSTRACT

A model of the high-frequency impedance of metal-ferroelectric-semiconductor structures has been composed and analyzed. An algorithm is formulated for recovering the impedance of the potential drop across the ferroelectric layer, band bending in a semiconductor, the total concentration of charged boundary states and minority charge carriers on the semiconductor surface from the experimental field characteristics as a function of the voltage across the structure. The results of high-frequency measurements of the capacitance and conductivity of Ni–$Ba_{0.8}Sr_{0.2}TiO_3$–Pt and Ni–$Ba_{0.8}Sr_{0.2}TiO_3$–Si structures in the paraelectric phase are presented. It is shown that Si does not evolve into a state of strong depletion in the entire range of external voltages, and the capacitances of the semiconductor and the metal-ferroelectric-silicon structures practically coincide. This is due to the almost complete screening of the ferroelectric layer polarization by the charges of electron traps at the $Ba_{0.8}Sr_{0.2}TiO_3$–Si contact. It is proposed to use dangling bond passivation methods realized in planar silicon technology to reduce the concentration of active trapping centers at the ferroelectric-semiconductor interface.

1. Introduction

For several decades, alternatives to insulating silicon oxide layers in electronic devices have intensely been searched and ferroelectric films were one of the priority areas [1]. Unique physical properties of ferroelectric materials (such as the high dielectric constant variable under the action of an external electric field) make it possible to create new types of information storage and processing devices on the basis of planar technology [2]. Solid solutions of barium-strontium titanate ($Ba_xSr_{1-x}TiO_3$ or BSTO) appeared to be a promising type of ferroelectric ceramics for practical applications until the beginning of the second decade of the 21st century. The BSTO retain ferroelectric properties above the room temperature and their dielectric constant remains high and in the paraelectric phase. However, despite studies of BSTO films began at the end of the last century [3,4], there are still no reports on transistor structures based on these ferroelectrics with working conducting surface channels of minority charge carriers in a nanometer range semiconductor [5]. After the start of the development of hafnium oxide as a ferroelectric insulating layer [6], it was considered that this material is the most promising for the creation of FeRAM (ferroelectric random-access non-volatile memory) cells [5]. However, the important performance characteristics of BSTO such as high dielectric constants of hundreds of units, low dielectric losses, low leakage currents, virtually no fatigue and material aging effects forced us to return to the problems of channel formation with a given material for the insulating layer. In this respect, an urgent physical task is to establish the reasons for not opening the conducting channels under the field electrode of metal-BSTO-Si structures and possible ways of overcoming these obstacles.

The most widespread are studies of the conducting and dielectric properties of metal-insulator-semiconductor structures by measuring the field dependences of their high-frequency impedance [7]. Summarizing the results obtained to date, one could assert that the features of high-frequency capacitance-voltage characteristics (CVC) which are anomalous compared to those of metal-SiO_2-Si objects are observed in metal-BSTO-Si structures. Externally, the shape of these characteristics is similar to the curve for silicon oxide structures: the transition between two plateaus (see Fig. 1). For metal-SiO_2-Si samples [7], a higher plateau is associated with a significant enrichment of the semiconductor, and the value of its capacitance C_{max} practically coincides with the capacitance

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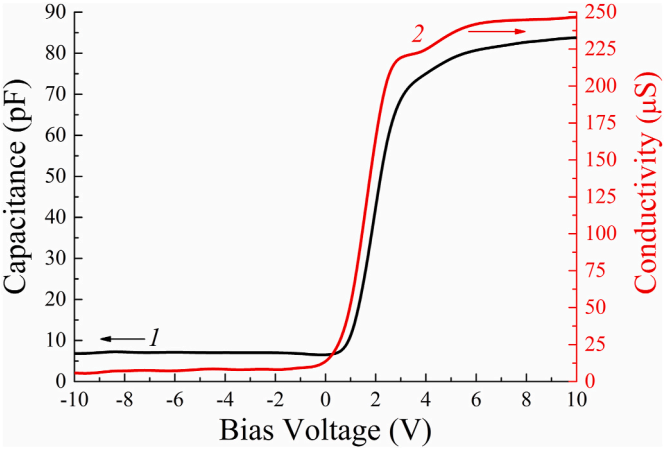

Fig. 1. Capacitance-voltage (curve 1) and conductivity-voltage (curve 2) characteristics of Ni-BSTO-Si structures at 121 °C.

of the SiO_2 layer. The lower plateau corresponds to a deep depletion of the semiconductor with the Fermi level pinning due to the generation of minority charge carriers (opening channel). Here, the capacity C_{min} coincides with the capacity of the semiconductor. The difference in capacitance values at different plateaus is several orders of magnitude. The capacity value on the upper plateau of metal-BSTO-Si samples is only several times, up to an order of magnitude, higher than on the lower one, and this is independent of the type of free charge carriers in the silicon substrate. Moreover, the nature of the plateau is not clear since the CVC of the ferroelectric layer has a bell-shaped shape (see Fig. 2) and the capacitance decreases several times with an increase in the voltage modulus. In this work, the contradictions mentioned above will be resolved, an explanation to the features and shape of the CV characteristics of metal-BSTO-Si structures is given, the reason for the non-opening of the minority carrier channel in silicon is revealed, and the ways of eliminating these obstacles are discussed.

There are three important points to note. First, the spontaneous polarization spatially distributed over domains does appear in the ferroelectric phase of the material [8]. Therefore, the expression for the dependence of the capacitance of a ferroelectric film on the applied voltage should be based on the three-dimensional averaging of the domain polarization over space. There is no spontaneous polarization in the paraelectric phase, and the problem of considering the polarization distribution over space becomes one-dimensional [9]. Hence, it is easier

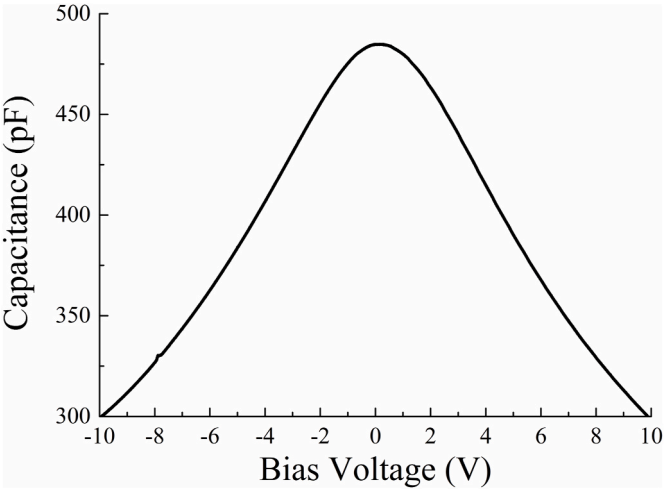

Fig. 2. The capacitance-voltage characteristic of Ni-BSTO-Pt structures at 121 °C.

to compare the experimental high-frequency impedance of BSTO films with theoretical concepts for the paraelectric phase. Second, high values of the effective dielectric constant of BSTO (which are hundreds of times higher than that of SiO_2) lead to an analogy between BSTO structures with ferroelectric layer thicknesses of hundreds of nm and silicon samples with thicknesses of tens of Å. As is known Ref. [10], high-frequency measurements show effects of the conductivity of the substrate and the insulating layer for ultrathin SiO_2 films. Naturally, similar behavior should be expected for BSTO-based structures. Thirdly, the widespread two and more frequency measurement methods for the analysis of ultrafine silicon oxide samples [11,12] are not suitable for BSTO based materials, since the conductivity of ferroelectric ceramics changes significantly with the frequency [13].

1.1. High-frequency impedance of metal-ferroelectric-semiconductor structures

Let us begin with a rigorous consideration for the paraelectric phase of the insulating layer of the metal-ferroelectric-Si structure. The band diagram of this structure with BSTO as the dielectric gap and with a Ni field electrode is shown in Fig. 3 for the semiconductor depletion (Fig. 3a) and enrichment states (Fig. 3b). Note that the equilibrium of the system (external voltage $V_g = 0$) is achieved in the state of depletion of the semiconductor if to not take into account the charges in the interfacial layer (IL) between silicon and BSTO. As follows from Fig. 3, the injection of electrons from silicon into the BSTO layer takes place in a state of sufficient enrichment of the semiconductor. This case corresponds to the upper plateau of CV characteristics where the high-frequency capacitance of the insulating layer C_{SE} is of the order of the geometric one, $\frac{æS}{4\pi h}$, where h and æ are the thickness and effective dielectric constant of the ferroelectric, respectively, and S is the structure area [14]. Under conditions of depletion of silicon, the ferroelectric film is electron deficient. In this case, the contribution of the recharge of the BSTO layer under a bias change into the C_{SE} value will manifest itself in the vicinity of the voltage $V_{SE} = 0$ (V_{SE} is the potential difference between the ceramic surfaces) in a narrow voltage interval compared to the measurement range for the paraelectric phase [15]. In the remaining main part of the characteristic, there is a regime of quasi-uniform polarization of the ferroelectric film and the function $C_{SE}(V_{SE})$ does not depend on the contact conditions [15]. This fact makes it possible to use in the analysis of high-frequency characteristics of the impedance of metal-BSTO-Si structures the function measured on metal-BSTO-metal structures with the same ferroelectric layer as the given one. Note that the conductivity of the insulating gaps σ_{SE} of the metal-BSTO-semiconductor and metal-BSTO-metal structures with the same ferroelectric thickness measured under the same deposition conditions differ from each other, which is due to the formation of different Schottky barriers at the ceramics-metal and ceramics-silicon contacts.

The reverse impedance of a one-dimensional layer structure is the sum of complex resistances of the each layer:

$$(i\omega C + \sigma)^{-1} = (i\omega C_{SE} + \sigma_{SE})^{-1} + (i\omega C_s)^{-1} + R_b. \quad (1)$$

here i is an imaginary unit; C and σ are the measured capacity and conductivity of the sample, respectively; ω is the cyclic frequency of the testing signal; C_s is the capacitance of the charged silicon region adjacent to the BSTO; R_b is the resistance of the Si substrate. Equation (1) does not contain the capacitance and conductivity of the transition interfacial layer between BSTO and silicon (see Fig. 3). The process of deposition of ferroelectric ceramics onto a substrate occurs at a temperature of about 600 °C in atmospheric conditions. Therefore, an IL layer is always formed due to the natural oxidation of silicon even on a pre-cleaned Si surface. The thickness of this layer is usually several nm and its high-frequency capacitance and conductivity do not make a significant contribution to the impedance of the structure. However, there are a large number of electron traps in the interface layer, and their

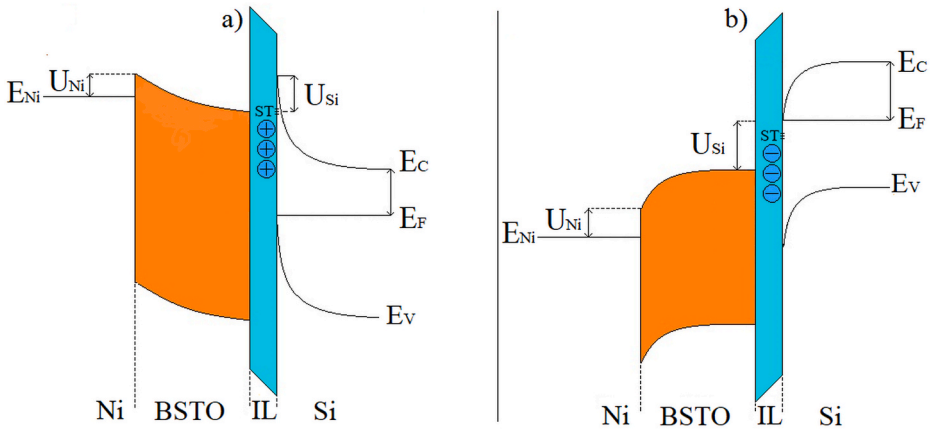

Fig. 3. Band diagram of the metal-BSTO-Si structure. (a) – the depletion state of the semiconductor; (b) – the enrichment state of the semiconductor. E_c is the bottom of the conduction band of silicon, E_v is the top of the valence band of silicon, E_F is the Fermi energy of electrons in a semiconductor, E_{Ni} is the Fermi level in a metal, U_{Ni} is the height of the conduction band of ceramics above the Fermi level in nickel, U_{Si} is the difference between the electron affinity energies of a ferroelectric and silicon, *ST* denotes surface electron traps, IL denotes interface layer between silicon and ferroelectric. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

recharging with a change in the stationary bias significantly affects the distribution of the external voltage over the sample.

Separating equality (1) into real and imaginary parts leads to relations:

$$\begin{gathered}\frac{\sigma}{\omega^2C^2+\sigma^2}=\frac{\sigma_{SE}}{\omega^2C_{SE}^2+\sigma_{SE}^2}+R_b,\\ \frac{1}{\left(C+\frac{\sigma^2}{\omega^2C}\right)}=\frac{1}{C_{SE}\left(1+\frac{\sigma_{SE}^2}{\omega^2C_{SE}^2}\right)}+\frac{1}{C_s}\end{gathered}\tag{2}$$

Conditions for values and formulas for the measured capacitance and conductivity of the metal-BSTO-semiconductor structure which follow from these relations are:

$$\begin{gathered}\frac{\sigma}{\omega^2C^2+\sigma^2}-R_b\geq 0,\\ \frac{1}{C_s}<\frac{1}{\left(C+\frac{\sigma^2}{\omega^2C}\right)}\leq\frac{1}{C_{SE}}+\frac{1}{C_s}\end{gathered}\tag{3}$$

$$C=\frac{C_s\left[\sigma_{SE}^2+\omega^2C_{SE}(C_{SE}+C_s)\right]}{\left(\sigma_{SE}-\omega^2R_bC_sC_{SE}\right)^2+\omega^2(C_{SE}+C_s+C_sR_b\sigma_{SE})^2}\tag{4}$$

$$\sigma=\frac{\omega^2C_{SE}^2\left[\sigma_{SE}(1+\rho_b\sigma_{SE})+\omega^2\rho_bC_{SE}^2\right]}{\left(\sigma_{SE}-\omega^2\rho_bC_sC_{SE}\right)^2+\omega^2(C_{SE}+C_s+C_s\rho_b\sigma_{SE})^2}\tag{5}$$

To eliminate the unknown variable σ_{SE}, one can express its value from the second equality in Eq. (2):

$$\sigma_{SE}=\omega C_{SE}\left[\frac{\frac{1}{C_{SE}}+\frac{1}{C_s}-\frac{1}{\left(C+\frac{\sigma^2}{\omega^2C}\right)}}{\frac{1}{\left(C+\frac{\sigma^2}{\omega^2C}\right)}-\frac{1}{C_s}}\right]^{1/2}\tag{6}$$

and substitute the resulting expression into the first equality in Eq. (2):

$$\begin{gathered}\frac{\sigma}{\omega C}-R_b\omega\left(C+\frac{\sigma^2}{\omega^2C}\right)=\\ =\left\{\left[1-\frac{\left(C+\frac{\sigma^2}{\omega^2C}\right)}{C_s}\right]\left[\frac{\left(C+\frac{\sigma^2}{\omega^2C}\right)}{C_{SE}}+\frac{\left(C+\frac{\sigma^2}{\omega^2C}\right)}{C_s}-1\right]\right\}^{1/2}\end{gathered}\tag{7}$$

Equation (7) does not contain an unknown function $\sigma_{SE}(V_{SE})$ and can be used for determining the distribution of the external voltage V_g over the insulating layer and semiconductor:

$$V_g=V_{SE}+V_s+\frac{U_{Ni}+U_{Si}-E_F}{q}\tag{8}$$

here V_s is the band bending in the semiconductor, q is the elementary charge, U_{Ni} is the height of the conduction band of the ceramic above the Fermi level in nickel, U_{Si} is the difference between the electron affinity energies of the ferroelectric and silicon, and E_F is the Fermi energy of electrons in the semiconductor (see Fig. 3). In expression (8), we neglected the drop in the external voltage across the IL layer due to its smallness. Necessary conditions for the existence of a solution are given by inequalities (3). Note that it is possible to determine the conductivity σ_{SE} from the first equality in Eq. (2), then substituting the obtained value into the second relation of Eq. (2). The result would be a formula for the capacity C_s expressed through variables C, σ and C_{SE} from equation (7). It is necessary to supplement Eqs. (7) and (8) with the condition for the electric induction D in BSTO at the interface with silicon:

$$-\frac{D}{4\pi q}=\frac{Q_s}{q}+p_{sq}\tag{9}$$

here Q_s is the charge per unit area in a semiconductor associated with the flow of free electrons (to be specific, we assumed that the silicon substrate is of the *n*-type), p_{sq} is the total concentration of the charge of electron traps in the IL layer and holes in Si at the contact with BSTO expressed in cm^{-2}. The function $p_{sq}(V_g)$ describes the recharge of the Si-BSTO interface when the external voltage changes.

One can formulate an algorithm for constructing dependencies $V_{SE}(V_g)$, $V_s(V_g)$ and $p_{sq}(V_g)$ from experimental characteristics $C(V_g)$, $\sigma(V_g)$ and $C_{SE}(V_{SE})$. For each voltage V_g, values $\left(C+\frac{\sigma^2}{\omega^2C}\right)$ and $\left[\frac{\sigma}{\omega C}-R_b\omega\left(C+\frac{\sigma^2}{\omega^2C}\right)\right]$ are calculated and the desired voltage V_{SE} at which the left and right sides of Eq. (7) are as close to each other as possible can be found, for example, by the brute-force method. For each V_{SE} value in this cycle, the V_s value can be found using Eq. (8), and the capacity and charge of the semiconductor are determined by expressions from classical statistics [7]:

$$\begin{gathered}C_s=S\left(\frac{æ_sq^2N_d}{8T\pi}\right)^{(1/2)}\frac{|1-e^{-\nu_s}|}{(e^{-\nu_s}+\nu_s-1)^{(1/2)}},\\ \frac{Q_S}{q}=\left(\frac{æ_sTN_d}{2\pi q^2}\right)^{(1/2)}(e^{-\nu_s}+\nu_s-1)^{(1/2)}\begin{cases}1, & \nu_s>0\\ -1, & \nu_s<0\end{cases},\\ E_F=T\ln\frac{N_c}{N_d}\end{gathered}$$

where $\nu_s=-\frac{qV_s}{T}$ is the dimensionless band bending in a semiconductor, $\nu_s>0$ at the silicon surface depletion; S is the field electrode area; $æ_s$ and N_d are the dielectric constant and donor concentration in Si, respectively; T is the absolute temperature in energy units; N_c is the effective density of states in the semiconductor conduction band. In accordance with the data of Ref. [16], the values of the barriers are $U_{Ni}=0.05$ eV

and $U_{Si} = 0.8$ eV. At pre-breakdown voltages for the electric induction D, one can use the relation obtained earlier[15]:

$$D = \frac{(k+1)}{h} \times \left\{ 1 + \frac{(k+4)}{3(k+3)} \left[\frac{C_{SEmax}}{C_{SE}(V_{SE})} - 1 \right] \right\}^{-1} \times \times (V_{SE} - V_{SEmax}) \quad (10)$$

where V_{SEmax} and C_{SEmax} are values of the voltage and capacitance of the metal-BSTO-metal structure at the CVC maximum; $(4\pi/k)$ is the inverse BSTO susceptibility; the k corresponds to the value derived from the formula for a flat capacitor: $C_{SEmax} = S(k+1)/4\pi h$. Note that strictly speaking the data obtained using the formulated algorithm will be valid in the regime of quasi-uniform polarization of a ferroelectric film that must be verified by comparing the experimental dependence $C_{SE}(V_{SE})$ for the Ni-BSTO-Pt structure with the formulas in Ref. [15].

1.2. Analysis of the characteristics of the Ni–$Ba_xSr_{1-x}TiO_3$–Pt and Ni–$Ba_xSr_{1-x}TiO_3$–Si structures

Our experimental studies were carried out using Ni-BSTO-Pt and Ni-BSTO-Si samples with the field electrode area $S = 2.7 \times 10^{-4}$ cm^2. Substrates used were n-type silicon, $N_d = 2.4 \times 10^{14}$ cm^{-3}, with a platinum sublayer or a natural oxide on the wafer surface. The choice of the electronic type of the substrate conductivity was due to wider possibilities of injection of main charge carriers from silicon into ferroelectric ceramics in comparison with the hole Si substrate. The concentration value N_d was calculated from the resistivity of the silicon substrate. A ferroelectric film with a thickness of $h = 330$ nm and a composition of $Ba_{0.8}Sr_{0.2}TiO_3$ was deposited by high-frequency sputtering of a polycrystalline target in an oxygen atmosphere using a Plasma-50SE installation (Russia). The thickness of the BSTO layer was determined using a SEM microscope FEI Nova NanoSEM 230 (USA). A more detailed description of the setup design and the film deposition technique can be found elsewhere [17,18]. Impedance measurements were carried out in the paraelectric phase in temperature range 110–130 °C and a frequency of 1 MHz using a high precision Agilent E4980A LCR meter, a portable computer with modified software, and a special chamber equipped with a thermostabilized heating stage. Details of the experimental setup were described previously [19].

Experimental results are shown in Figs 1 and 2 for measurement temperature 121 °C. Forms of curves for other temperatures are similar to those shown in these figures, and inequalities used below remain for measured characteristics. With the value of C_{SEmax}, the parameter value $k = 708$ was obtained using the formula for a flat capacitor. The analysis of Figs 1 and 2 leads to the relationship between the values of the experimental characteristics: $C_{SE} >> C$ and $(\sigma/\omega C) << 1$. The injection of electrons from Si into BSTO increases the capacity of the insulating layer, therefore, taking this circumstance into account will lead to an enhancement of the capacity inequality. Thus, the left side of equation (7) is much less than unity according to our experimental data. Correspondingly, it follows from the right-hand side of this equality that $\{1 - [(C + \sigma^2/\omega^2 C)/C_s]\} < 1$. Thus, the approximate equality is preserved in the entire voltage range:

$$C \approx C_s \quad (11)$$

The value of the semiconductor capacity is slightly greater than $(C + \sigma^2/\omega^2 C)$, and it is this small difference $C_s - C$ that ensures the fulfillment of conditions (3). Naturally, the results (11) it will obtained for the passage to the limit $C_{SE} \to \infty$ in expression (4). Another experimental fact (see Fig. 1) is that the proximity of capacitance values to each other at the lower CVC plateau $C_{min} = 7 \cdot 10^{-12}$ F and the semiconductor in the flat band state ($V_s = 0$) $C_{sfb} = 9.17 \cdot 10^{-12}$ F. According to the second inequalities (3), this means that the band bending of silicon is significantly limited: $\nu_s < 1$ with the depletion ($V_g < 0$) and $|\nu_s| < 5$ with the enrichment ($V_g > 0$). Thus, the major part of the external voltage falls on the ferroelectric layer:

$$V_{SE} \cong V_g - \frac{U_{Ni} + U_{Si} - E_F}{q} \quad (12)$$

The plateaus in the $C(V_g)$ and $\sigma(V_g)$ graphs are a consequence of the low sensitivity of the band bending in the semiconductor to a change in V_g. At the lower plateau, where the condition $\nu_s \approx const$ is more rigidly satisfied, the capacitance and conductivity depend weaker on voltage than at the upper plateau. The practical non-realizability of noticeable depletion of the semiconductor predetermines not opening the hole conduction channel in silicon with a decrease in the external voltage.

Such a response of the Ni-BSTO-Si structure to a change in the field voltage can only be explained by the recharge of surface electron traps (ST) in the interfacial layer. It follows from expressions (9), (10), and (12) that the ST charge per unit area p_{sq} of the sample changes from $+9,3 \cdot 10^{13}$ to $-9,3 \cdot 10^{13}$ cm^{-2} with an increase in voltage from −10 to 10 V. There is almost complete screening of the ferroelectric gap polarization in the metal-BSTO-Si structure by charges of electron traps in the IL layer. The high spatial ST concentration causes a high energy density of localized electronic states in the interfacial layer. To explain the reaction of our samples to a change in the bias, it should be assumed that the Fermi level in a semiconductor is in the vicinity of a local minimum of the ST energy density in the state of flat bands. An increase in the density of localized electronic states deep into the Si band gap should be steeper than towards the bottom of the conduction band. As is shown experimentally, then the Fermi level pinning in silicon will be more pronounced in the region of the lower CVC plateau (Si depletion) than the upper one (Si enrichment).

Note that results of (11) and (12) obtained in the analysis of our experiments did not require the use of the data processing algorithm formulated in the section “High-frequency impedance of metal-ferroelectric-semiconductor structures”. Due to the observed inequalities $C_{SE} >> C$ and $(\sigma/\omega C) << 1$ it turns out that the external voltage falls mainly on the ceramic insulator. In this case, the dependency $V_s(V_g)$, which allows us to build this algorithm, at this stage does not matter much and does not affect the main result of the work – the detection of almost complete shielding of the external voltage by traps. The function $V_s(V_g)$ will be needed in the development of this work in order to determine the spectral density of localized electronic states at the BSTO-Si contact. Summarizing, one can assert that the high density of active traps in the interphase layer of Ni-BSTO-Si structures causes a small difference in the capacitance values on the CVC plateau compared to metal-SiO_2-Si structures that does not allow silicon to be transferred into a state of deep depletion. This circumstance prevents the widespread use of applications based on such ferroelectrics. The IL layer consists mainly of silicon oxide and surface levels at the Si–SiO_2 interfaces correspond to paramagnetic states of Si atoms with an unpaired electron delocalized over three atoms in the semiconductor bulk $\equiv Si_3Si\bullet$, the so-called P_b centers or dangling bonds [20]. Theoretically, the concentration of these dangling bonds is $8 \cdot 10^{14}$ cm^{-2}, and they influence recharging during both depletion and enrichment of a semiconductor [20]. An analogy arises between our modern structures with a ferroelectric insulating layer and the metal-SiO_2-Si structures in the sixties and seventies of the last century when active traps at the silicon-oxide contact prevented the manufacture of high-quality transistors with a conduction channel for minority charge carriers. This problem was technologically solved by passivating the dangling bonds with hydrogen atoms. The emerged questions about the stability of such passivation to radiation and the action of a strong electric field gave rise to the development of a new direction of research; namely, the investigation of damages to metal-SiO_2-Si structures [21]. The work carried out before the tenth years of this century made it possible to solve the existing problems and create objects with the necessary resistance to external influences. Naturally, the elimination of obstacles to opening the conduction channel of minority charge carriers in a semiconductor of a Ni-BSTO-Si structure should be carried out by passivating traps in

the interfacial layer using the experience gained in planar silicon technology.

2. Conclusion

Strictly speaking, the developed methods for analyzing the high-frequency characteristics of the impedance of metal-ferroelectric-semiconductor structures are applicable in the case of the paraelectric phase of the insulating gap. However, the main physical result of this work is the establishment of almost complete screening of the polarization of the ferroelectric layer by ST charges in the interphase layer at the BSTO-Si contact goes beyond phase restrictions. A high concentration of recharging localized electronic states at the ferroelectric-semiconductor interface should prevent the formation of domains in a sample, at least near the contact surface. It is possible that this fact is related to the explanation of the specific features of the field characteristics of the high-frequency impedance: for the structures with the thicknesses of insulating layers of hundreds of nm and thinner, the external form of the CV characteristics in the paraelectric and ferroelectric phases is practically the same. As for the prospects for using ferroelectric ceramics $Ba_xSr_{1-x}TiO_3$, there are hopes for the use of dangling bond passivation methods implemented in planar silicon technology. This would make it possible to drastically reduce the concentration of rechargeable electron traps in the interphase layer of metal-BSTO-Si structures and return this material to the category of promising FeRAM cells for the creation of non-volatile memory cells.

Credit author statement

Evgeny I. Goldman: Conceptualization, Writing - original draft, Writing - review and editing;

Galina V. Chucheva: Conceptualization, Supervision, Writing - review and editing;

Dmitry A. Belorusov: Investigation, Writing - original draft.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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