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SEMICONDUCTOR STRUCTURES, LOW-DIMENSIONAL SYSTEMS, AND QUANTUM PHENOMENA

Features of the Characteristics of Field-Resistant Silicon–Ultrathin Oxide–Polysilicon Structures

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Abstract—Results of studying the features of the current–voltage (I–V) and capacitance–voltage characteristics of field-resistant silicon–ultrathin oxide–polysilicon structures are presented. It turns out that the total recharging of localized electron states and minority carriers concentrated near the substrate–insulator interface, which occurs with a variation in the field voltage, is an order of magnitude higher than that of samples susceptible to damage by the field stress effect. The tunneling I–V characteristic is significantly asymmetric; notably, the current flowing from the field electrode into the silicon substrate is several orders of magnitude lower when compared with the current flowing from silicon to polysilicon at identical external voltages dropping across the insulating layer. To explain this asymmetry, it is assumed that a potential barrier in the transition layer from polysilicon to oxide, which separates the semiconductor electrode and substrate, has a height of ~1 eV and therefore always hinders electrical transport; for reverse currents, this barrier stops limiting the conductivity as soon as the tunneling level becomes higher than it.

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Electric fields which appear under controlling effects in ultrathin insulating layers of nanoscale active elements of modern semiconductor devices reach several units of 10^6 V/cm. The effect of such a strong although prebreakdown electric field on n-Si–SiO_2 structures generates several processes of different intensities in silicon-oxide films. First, this is electron capture from the semiconductor and the gate by Si–O bonds located along the electric force lines. This phenomenon results in a substantial decrease in the activation energy for the thermal detachment of a negatively charged oxygen atom from silicon and thereby the formation of oxygen vacancies in the oxide. It is currently considered that the accumulation of these vacancies with time and their joining into lines that shorten the controlling electrode and semiconductor base is the main mechanism of breakdown development in the insulating layer of metal–oxide–semiconductor (MOS) structures [1–3]. Second, hydrogen present in SiO_2 transfers to oxide surfaces and reacts with passivated and unpassivated dangled bonds at Si–SiO_2 interfaces, and the concentration of surface electron traps, so-called P_b centers, increases in connection with this [4–6]. Third, built-in charge accumulates near the Si–SiO_2 interface. It is associated both with the redistribution of ions over the oxide and the recharging of localized electron states that are present and generated under the field effect. The listed phenomena are accompanied by an increase in the conductivity through the insulating layer both due to the formation of new channels—the formation of short (not through) lines of oxygen vacancies and an increase in the role of tunneling through electron states in the oxide (trap-assisted current)—and in connection with an additional electric field due to the accumulation of built-in charge [2]. From the viewpoint of the variation in the properties of the Si–SiO_2 contact, the consequences of the mentioned processes can be separated into reversible ones, so-called "oxide damage", and irreversible, soft breakdown and breakdown of the insulating layer. We note that despite the prebreakdown values of the electric fields under consideration, the probability of sample transfer to the irreversible soft breakdown state appears with an increase in the duration of the effect [2, 3].

Our group have studied variations in the properties of ultrathin (<5 nm) silicon oxides after the damage of MOS structures in electric fields for several years [7–9]. It turns out that there is a group of samples, in which the reaction of the "damage" type to the field effect is almost lacking, i.e., both the conductivity through the oxide and the distribution of the built-in charge barely vary with an increase in the holding time under field voltages of different polarities up to the transition to the soft breakdown state. In this work, we will consider the features of the characteristics of such objects. The parameters of the investigated samples

are the same as the parameters of objects, in which the "damage" phenomenon was observed [7, 8]: these are MOS structures of Si with an Al–n^+-Si:P field electrode (the donor concentration in polysilicon $N_d^+ \approx 10^{20}$ cm^{-3}, area $S = 1.6 \times 10^{-3}$ cm^2) insulated from the (100) n-Si substrate by a layer of pyrogenic oxide with an optical thickness of ~4 nm. The structures were subjected to the field stress effect at room temperature at the same field voltages V_g as in the case of studying the damage of ultrathin SiO_2 [7, 8]: $V_g = -3.8$ V (substrate depletion), the minimal holding time is 16 min; and $V_g = 3.2$ V (substrate enrichment), the minimal holding time is 20 min. We measured the current–voltage (I–V) characteristics and high-frequency capacitance–voltage (C–V) characteristics of the objects at frequencies of 1 and 0.5 MHz (capacitances C_1 and C_2) using an LCR Agilent E4980A precision meter [9]. So that the values of the high-frequency capacitances and current would correspond to the same sample state, the experiments were performed as follows: the specified field voltages were supplied to the sample for each measurement point from position $V_g = 0$, the current was recorded after the end of the RC processes (time <0.1 s), and then the capacitances C_1 and C_2 were recorded for 3 s. After this, the supplied voltage V_g was reduced to zero and the structure was held for 6 s. The total duration of the current and capacitance measurements for the same voltage across the field electrode (6 s) is substantially shorter than the characteristic time of the transient process associated with the recharging of localized electron states at the Si–SiO_2 interface (>100 s). Such a procedure allows us to minimize the sample residence duration under stress conditions during measurements. These high-frequency C–V characteristics, which correspond to two high frequencies, allow us to determine the donor concentration N_d near the Si–SiO_2 interface, the resistance of the semiconductor substrate R_b, and the field-voltage dependences of the following quantities: band bending in the semiconductor V_s, the external voltage drop V_s across the insulating layer, and the total density of the built-in charge and charge of interface states and holes at the interface p_{sq} expressed in cm^{-2} [8, 10].

Figure 1 shows the field dependences of the capacitance $C(V_g)$ of the sample measured in the state before the field stress effect at room temperature at two frequencies. Their variations after field effects of different polarities and holding time did not exceed 2% in contrast with the objects in [8], where a decrease in the capacitances by a factor of several times was recorded after the field effect. A similar pattern was also observed with respect to currents through the insulating layer: the I–V characteristics shifted no larger than hundredths of a volt after sample holding in a strong field. Processing of the high-frequency C–V characteristic data according to the procedure described in [8, 10] gave the following: $N_d = 1.14 \times 10^{15}$ cm^{-3} and $R_b = 88$ Ω. These quantities are similar to the values determined in [8]. The dependence $p_{sq}(V_g)$ is presented in Fig. 2. It is seen that the recharging scale of the Si–SiO_2 interface in these objects is higher by an order of magnitude when compared with damaged structures [8, 11]: the increase in p_{sq} was $\Delta p_{sq} = 1.4 \times 10^{13}$ cm^{-2} upon varying V_g from –0.5 to –6 V. It turned out at the field voltage depleting semiconductor that $V_i \propto V_g/2$. This fact means that the sample is in the time-dependent state and in the nonequilibrium state with respect to minority carriers (hole generation delays) for these V_g. Figure 3 shows the logarithmic dependences of the current branches through the oxide on the external voltage drop across the insulating layer $\varphi_\pm(V)$. Here, $V = V_g$ at $V_g > 0$ and $V = -V_i$ at $V_g < 0$; $\varphi_+(V) = \log[I(V_g)/I\big|_{V_g=1\,\mathrm{V}}]$ for $V_g > 0$ and $\varphi_-(V) = \log[I(V_i)/I\big|_{V_i=-1\,\mathrm{V}}]$ for $V_g < 0$, and I is the current in the field electrode–substrate circuit. Normalization of the current $I\big|_{V_g=1\,\mathrm{V}}$ and $I\big|_{V_i=-1\,\mathrm{V}}$ were selected starting from the fact that these values of the voltages and currents are approximately equal modulo: $I\big|_{V_g=1\,\mathrm{V}} = 5.6 \times 10^{-12}$ A and $I\big|_{V_i=-1\,\mathrm{V}} = -4.8 \times 10^{-12}$ A. The I–V characteristics presented in Fig. 3 correspond to tunneling transfer through an insulating barrier. To verify this assumption, the time dependences of the current and capacitances were measured at frequencies of 1 and 0.5 MHz for several V_g. Recharging currents $qS(dp_{sq}/dt)$ calculated on this basis (q is the elementary charge and t is time) turned out to be 1.5–2 orders of magnitude smaller than I modulo. It follows from Fig. 3 that there is strong asymmetry of the tunneling I–V characteristic with respect to the polarity of the voltage dropping across the insulator. The characteristics $\varphi_+(V)$ and $\varphi_-(V)$ are approximately identical for voltages $V < 1$; on the contrary, the current rise slope at $V > 1$ at positive values is 2–3 orders of magnitude higher than at negative values: $I = 2 \times 10^{-8}$ A at 3 V across the oxide and $I = -1.6 \times 10^{-10}$ A at –3 V. Such behavior of the I–V characteristics should not be typical of silicon MOS structures with an ultrathin oxide, where the asymmetry in the direct tunneling conditions can be associated with the difference in the Fermi energies in semiconductors on different sides relative to the insulator and, therefore, it should be pronounced relatively weakly. The experimental dependences $I(V_g)$ presented in Fig. 15.12 of review [2] confirm the irregularity of the curves presented in Fig. 3. We note that the asymmetry of the I–V characteristics corresponding to a different field-voltage polarity and described in this work differs from that one considered in [12]. In this article, the situation when the current flowing from a field electrode to

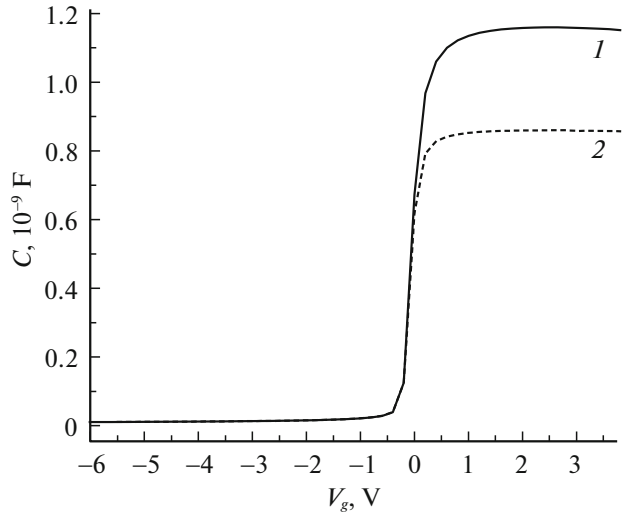

Fig. 1. High-frequency $C-V$ characteristics $C(V_g)$ of a silicon MOS structure at frequencies of (*1*) 0.5 and (*2*) 1 MHz.

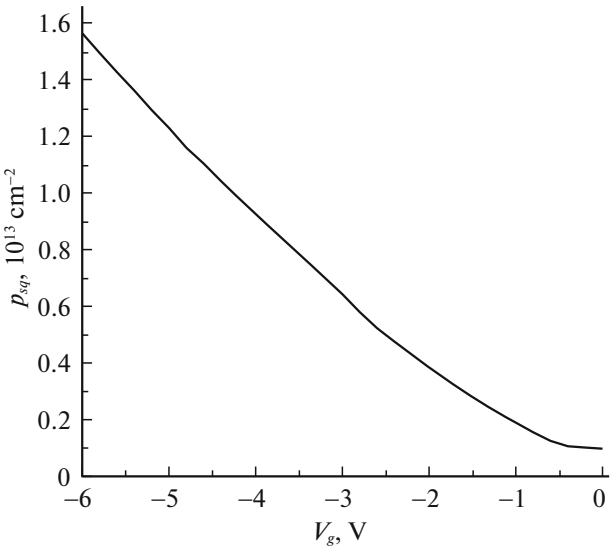

Fig. 2. Field-voltage-V_g dependence of the total density of the built-in charge, charge of interface states, and holes at the substrate–oxide contact p_{sq}.

a semiconductor at small V_g was smaller than the current flowing from silicon to a field electrode was analyzed; however, this effect disappeared with an increase in the voltage.

The transition layers between crystalline silicon and its oxide occupy no less than 40% of the volume of an ultrathin insulator [13]. In fact, these layers are important components of the oxide structure, in many aspects determining its properties. Therefore, the potential barrier of the insulating interlayer has a much more complex shape than rectangular [14]. Since the formation of transitions from the substrate to the oxide and from the oxide to polysilicon occurs in different manufacturing processes, we should also expect different (asymmetric) shaped dependences of the potential on the coordinate at these contacts. This fact means that the transition from SiO_2 to polysilicon should be wider than on the silicon-substrate side. In this context, we add that the shape of the coordinate dependence of the potential should also be affected by the polycrystallinity of the field electrode. To explain the above-described asymmetry of the tunneling $I-V$ characteristics of silicon MOS diodes, it is sufficient to assume that the potential structure in the insulator contains a branch in the transition layer on the polysilicon side growing with the removal from semiconductor, which transfers to the main high barrier extending to the contact with the silicon substrate at a height of ~1 eV. Such a branch in addition to the main barrier will always hinder electrical transport from the field electrode to the substrate, while for the reverse flow, it will stop affecting the conductivity as soon as the tunneling level passes above it.

This work opens up a series of investigations into the nature of the stability of samples to damaging field effects and the revelation of a possible connection between this property and the potential barrier structure in an insulating layer and other characteristics of silicon MOS structures with an ultrathin oxide. The next step is the construction of the actual potential relief separating a semiconductor and field electrode based on the procedure developed in [14]. The solution to this problem will give an answer to the validity of the above assumption on the shape of the insulating

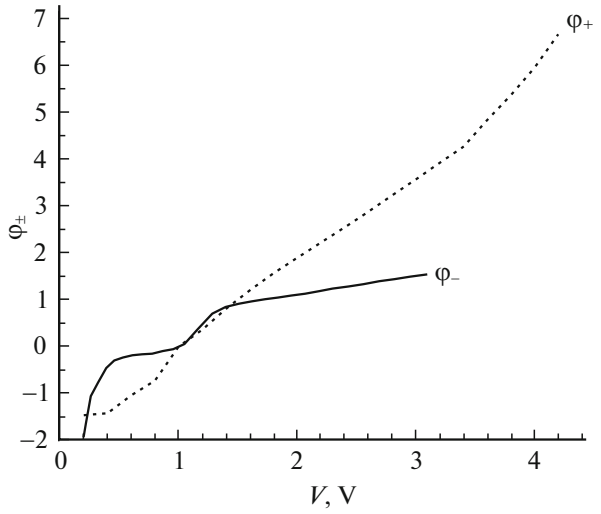

Fig. 3. Logarithmic form of the tunneling $I-V$ characteristics of the insulating layer of the silicon MOS structure. $\varphi_+(V) = \log[I(V_g)/I\big|_{V_g=1\,\mathrm{V}}]$ for $V_g > 0$ and $\varphi_-(V) = \log[I(V_i)/I\big|_{V_i=-1\,\mathrm{V}}]$ for $V_g < 0$.

barrier allowing explanation of the asymmetry of the observed tunneling I–V characteristics.

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