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SURFACES, INTERFACES, AND THIN FILMS

Generation of Surface Electron States with a Silicon–Ultrathin-Oxide Interface under the Field-induced Damage of Metal–Oxide–Semiconductor Structures

E. I. Goldman, S. A. Levashov, V. G. Naryshkina, and G. V. Chucheva*

Kotelnikov Institute of Radio Engineering and Electronics, Russian Academy of Sciences (Fryazino Branch), Fryazino, Moscow region, 141120 Russia

**e-mail: gvc@ms.ire.rssi.ru*

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Abstract—The high-frequency capacitance–voltage characteristics of metal–oxide–semiconductor structures on *n*-Si substrates with an oxide thickness of 39 Å are studied upon being subjected to damage by field stress. It is shown that the action of a high, but pre-breakdown electric field on an ultrathin insulating layer brings about the formation of a large number of additional localized interface electron states with an energy level arranged at 0.14 eV below the conduction band of silicon. It is found that, as the field stress is increased, the recharging of newly formed centers provides the accumulation of excess charge up to 8×10^{12} cm^{-2} at the silicon–oxide interface. The lifetime of localized centers created under field stress is two days, after which the dependences of the charge localized at the semiconductor–insulator interface on the voltage at the gate after and before field stress are practically the same.

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1. INTRODUCTION

The effect of a high, but pre-breakdown electric field on silicon-oxide layers results in so-called damage of the insulators. This damage manifests itself as an increase in the tunneling conductivity of the insulators and an increase in the concentration of localized electron states at the semiconductor–insulator interface [1]. Studies of these phenomena in relatively thick (>5-nm-thick) SiO_2 layers have been conducted for more than 40 years [2], and to date, sufficiently comprehensive concepts of the mechanisms of the observed effects have been developed [3–6]. The engineering of nanoscale electronic devices stimulated studies of the damage of thin and especially ultrathin (<4-nm-thick) insulating films. The results obtained in this context describe mainly an increase in the tunneling conductivity of the oxide due to the accumulation of additional built-in charge under field stress [1–7]. The formation of hole-generation centers under the field-induced damage of silicon-based metal–oxide–semiconductor (MOS) structures with an oxide thickness of ~40 Å was considered in [8]. Actually, from analysis of the dynamic current–voltage characteristics of the sample after stress, an increase in the generation rate of minority charge carriers in the depletion state of the interface was established. Direct data on the band bending in the semiconductor, the change in the charge of interface states, and the concentration of minority charge carriers near the interface can be obtained from the high-frequency capacitance characteristics of metal–insulator –semiconductor structures [9]. In this paper, we report the results obtained by measuring the high-frequency capacitances of *n*-Si–MOS structures in the dynamic mode of studies.

There are some specific features of studies of the properties of semiconductor–insulator interfaces by analyzing the field dependences of the high-frequency capacitance of structures with ultrathin insulating layers in comparison with studies of structures with relatively thick layers [10]. First, it is necessary to take into account the possible contributions of the conductivity of the semiconducting substrate, the tunnel currents throughout the oxide, and the processes of the generation of minority charge carriers. Second, it is necessary to carry out highly precise measurements and to use noise-smoothing methods of experimental data processing. We performed experiments using *n*-Si–MOS structures similar to those used in [11]. In [11], it is shown that the value of the active component of the impedance of these samples is beyond the region of allowed measurements and, among the specific features of ultrathin insulators, only the resistance of the semiconductor part manifests itself in the capacitance

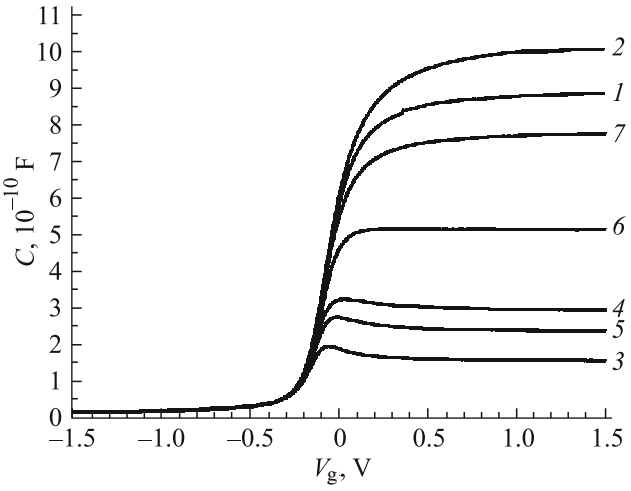

Fig. 1. High-frequency capacitance–voltage characteristics obtained experimentally for the Si–MOS structure before and after field action: (*1*, *2*) before the stress at (*1*) 1 and (*2*) 0.5 MHz; (*3*) immediately after the stress at (*3*) 1 and (*4*) 0.5 MHz; (*5*, *6*) within 2 h after the stress at (*5*) 1 and (*6*) 0.5 MHz; and (*7*) within 4 h after the stress at 0.5 MHz. On the scale, the curves corresponding to the state within 2 days after the stress at 1 and 0.5 MHz merge together with curves *1* and *2*, respectively. The plot obtained by measurements 4 h after the stress at 1 MHz is practically coincident with curve *6*.

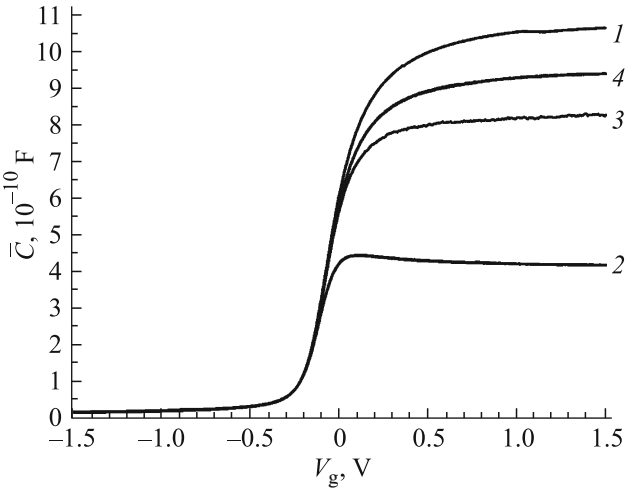

Fig. 2. High-frequency field dependences of the capacitance $\bar{C}(V_g)$: (*1*) before the stress, (*2*) immediately after the stress, and (*3*, *4*) within (*3*) 2 and (*4*) 4 h after the stress. On the scale, the curve corresponding to the state in 2 days after the stress merges with curve *1*.

characteristics. This means that it is sufficient to measure the field characteristics of the reactive component of the impedance of the sample only at two high frequencies and, from these data, to determine both the conductivity of the substrate [10, 12] and the capacitance of the charged surface region near the semiconductor–insulator interface.

The experiments were performed with the use of an LCR Agilent E4980A precision meter at the frequencies 0.5 and 1 MHz. The samples were *n*-Si–MOS structures with an oxide thickness of 39 Å and a field electrode area of $S = 1.6 \times 10^{-3}$ cm^2. The samples were subjected to field stress similarly to how it was done in [8]: the samples were kept at the voltage at the field electrode $V_g = -3.8$ V for 1 h at room temperature. Thus, at the polarity of V_g depleting the semiconductor, we took into account the delay of the field action on the insulator due to the slow accumulation of minority charge carriers (holes) near the interface and a partial drop in the external voltage at silicon in the steady state. The impedance of the structures was measured in the dynamic mode, the voltage V_g was varied with time with a constant rate of field scanning $\beta = 15$ mV s^{-1}, at first from 1.5 to -1.5 V (the forward branch) and then from -1.5 to 1.5 V (the reverse branch). Such limitation of the scan amplitude of the field stress prevented the sample from additional damage during recording of its capacitance. Figure 1 shows the capacitance–voltage characteristics of the samples $C_1(V_g)$ at 0. 5 MHz and $C_2(V_g)$ at 1 MHz in different stages before and after application of the stress. We assume that, for the frequencies, at which the measurements were conducted, the recharging of surface states and the generation–recombination of minority charge carriers have no time to respond to oscillations of the external voltage. The high-frequency capacitance $\bar{C}$ corresponding to the charged semiconductor surface layer and the insulating gap and the conductivity of the semiconductor substrate ρ_b were determined from experimental values of $C_1(V_g)$ and $C_2(V_g)$ in accordance with [10, 12] by the formulas

$$\bar{C} = \frac{C_1C_2(\omega_1^2 - \omega_2^2)}{\omega_1^2C_1 - \omega_2^2C_2},$$

$$\rho_b = \sqrt{\frac{(C_2 - C_1)(\omega_1^2C_1 - \omega_2^2C_2)}{\omega_1^2C_1 - \omega_2^2C_2}}, \quad (1)$$

Here, ω_1 and ω_2 are the circular frequencies of variations in the testing voltage.

The dependences $\bar{C}(V_g)$ are shown in Fig. 2. The curves corresponding to the forward and reverse branches are practically coincident and can be distinguished only in the region of hole generation which lags and manifests itself mainly in the reverse branch. The calculated dependence $\rho_b(V_g)$ has the form of a plateau with $\rho_b \approx 65\ \Omega^{-1}$; at negative voltages, the plateau transforms into a sharp peak with a maximum at $V_g = -0.26$ V. The peak is a nonphysical feature determined by the addition of all field voltages of all capacitance curves, which is responsible for errors in the calculations: formula (1) involves the square root of

Parameters V_g, $\left(\frac{qV_{sh}}{T}\right)^{1/2}$, and N_d calculated at different v_s

v_s	0	−1	−2	−3	−4
V_g, B	−0.199	−0.225	−0.258	−0.284	−0.312
$\left(\frac{qV_{sh}}{T}\right)^{1/2}$	9.764×10^{-2}	1.011×10^{-1}	9.62×10^{-2}	9.744×10^{-2}	9.745×10^{-2}
N_d, cm^{-3}	2.608×10^{15}	2.794×10^{15}	2.531×10^{15}	2.597×10^{15}	2.597×10^{15}

the difference between the capacitances that are two close quantities. The feature shape (peak) is defined also by a sharp deceleration of the decrease in the capacitances under variation in the voltage from −0.2 to −0.5 V (Fig. 1).

If quantum-confinement effects and the degeneracy of the electron system are disregarded, the relationship between band bending in the *n*-type semiconductor and the high-frequency capacitance $\bar{C}$ can be represented on the basis of classical formulas [9] as

$$\frac{\bar{C}}{C_i - C} = \left(\frac{qV_{sh}}{T}\right)^{(1/2)} (e^{-v_s} + v_s - 1)^{-(1/2)} |1 - e^{-v_s}|, \quad (2)$$

Here, C_i is the capacitance of the insulator layer, V_s is the voltage drop in the semiconductor, $v_s = -qV_sT^{-1}$ is dimensionless band bending in the semiconductor ($v_s > 0$ in the case of depletion and $v_s < 0$ in the case of enrichment), q is the elementary charge, T is the temperature expressed in energy units, $V_{sh} = \frac{2\pi\varepsilon_s q N_d h^2}{æ_i^2}$, ε_s and ε_i are, correspondingly, the permittivities of the semiconductor and insulator; h is the oxide thickness; and N_d is the dopant impurity concentration near the interface. The value of C_i was taken to be the value of $\bar{C}$ for the undamaged sample in the state of high enrichment of the semiconductor. In the process of high-temperature oxidation of the silicon surface and during purification of the resultant structures, the dopant concentration near the Si–SiO_2 interface can be changed compared to the concentration within the semiconductor-substrate bulk [13]. Therefore, the value of N_d or, more strictly, the value of the parameter V_{sh} must be determined directly from experimental data. In experiments at room temperature, the interface states are recharged practically to the flat-band state of the semiconductor. For this reason, the parameter V_{sh} must be calculated from the experimentally recorded dependences $\bar{C}(V_g)$ in the region of field voltages corresponding to slight enrichment of the semiconductor surface with free electrons: in this region, the interface states have already been practically filled and do not change their charge, as the field stress is increased, and quantum-confinement effects do not yet manifest themselves. In this range, the expression

$$\left(\frac{C_i}{C_i - C}\right)^2 \frac{2}{C}\frac{Td\bar{C}}{qdV_g} = \frac{(e^{-2v_s} + 2v_s e^{-v_s} - 1)}{(e^{-v_s} + v_s - 1)|1 - e^{-v_s}|}, \quad (3)$$

is satisfied, with the left-hand side being a function of the field stress only and the right-hand side depending only on the band bending of the semiconductor. From relation (3) with the specified values of $v_s = 0, -1, -2, -3$, and -4, we can determine the corresponding values of V_g. From the dependence $\bar{C}(V_g)$ at these values of V_g, we can calculate the sought-for value of the parameter $\left(\frac{qV_{sh}}{T}\right)^{(1/2)}$ in accordance with formula (2). Table lists the values of this parameter for the indicated values of the band bending of the undamaged sample and the corresponding values of the field stress and dopant concentration. In further calculations, we used the average values of $\left(\frac{qV_{sh}}{T}\right)^{(1/2)} = 9.796 \times 10^{-2}$ and $N_d = 2.625 \times 10^{15}$ cm^{-3}; the spread of the data was smaller than 1.7%.

The dependences of the dimensionless band bending in the semiconductor v_s and the quantity p_{sq} (p_{sq} expressed in cm^{-2} is the total charge of interface states and holes at the interface) on the voltage at the field electrode are shown in Figs. 3 and 4. The values of p_{sq} were calculated from the expression

$$p_{sq} = -\frac{C_i T}{Sq} \times \left[\frac{qV_g}{T} + v_s + 2\left(\frac{qV_{sh}}{T}\right)^{(1/2)} (e^{-v_s} + v_s - 1)^{(1/2)} Sgn v_s\right], \quad (4)$$

where

$$Sgn v_s = \begin{cases} 1, & v_s > 0, \\ -1, & v_s < 0. \end{cases}$$

Let us analyze the results. As can be seen from Fig. 1, the stress substantially lowers the levels of the sample capacitances, at which they flatten out at high positive field stresses. This is indicative of a sharp increase in the concentration of surface states. Filling

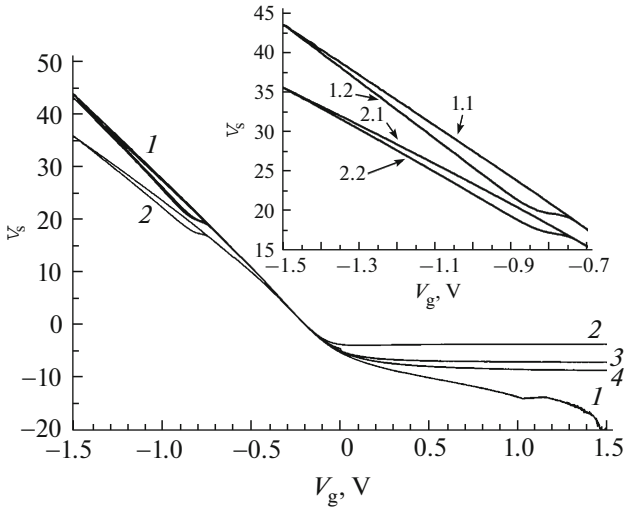

Fig. 3. Dependences of the dimensionless band bending in the semiconductor on the voltage at the field electrode (*1*) before the stress, (*2*) immediately after the stress, and (*3*, *4*) within (*3*) 2 and (*4*) 4 h after the stress. At negative V_g, curves *3* and *4* are practically coincident with curve *1*. The inset shows the dependences (*1.1*) before the stress (forward branch); (*1.2*) before the stress (reverse branch); (*2.1*) immediately after the stress (forward branch); and (*2.2*) immediately after the stress (reverse branch).

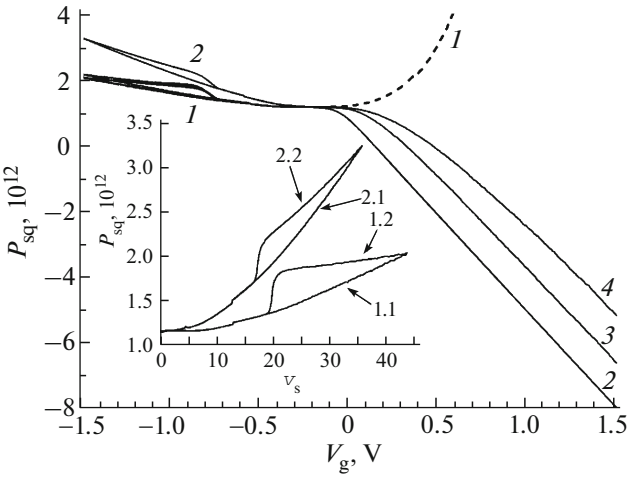

Fig. 4. Dependences of the total charge of interface states and holes on the voltage at the field electrode (*1*) before the stress; (*2*) immediately after the stress; and (*3*, *4*) within (*3*) 2 and (*4*) 4 h after the stress. At negative V_g, curves *3* and *4* are practically coincident with curve *1*. The inset shows the dependences (*1.1*) before stress (forward branch); (*1.2*) before stress (reverse branch); (*2.1*) immediately after the stress (forward branch); and (*2.2*) immediately after the stress (reverse branch).

of the states with electrons occurs upon pinning of the Fermi level, which means that the band bending in the semiconductor is nearly constant; therefore, at the plateaus, $\overline{C}$ (Fig. 2) is much smaller than C_i. The plots shown in Figs. 3 and 4 support this conclusion: at the plateau $v_s \approx -3.6$ and the number of negative charges reaches $p_{sq} = 8 \times 10^{12}$ cm^{-2}. Hence it follows that the electron energy level at these states is about $[T\ln(N_c/N_d) - 3.6]$ or 0.14 eV below the conduction band.[1] The curve $p_{sq}(V_g)$ for the undamaged sample (Fig. 4) is partially shown by a dashed line. This indicates the nonphysical character of the corresponding dependence in the region of high field stresses: the quantity p_{sq} is bound to be constant, whereas it increases with V_g. In the case of such enriching band bendings in the semiconductor, the effects of quantum confinement and degeneracy of the electron system become substantial. Therefore, expression (2) based on the classical concepts and Boltzmann statistics gives incorrect values of the calculated quantities in this region of V_g. In support of the results of [8], it should be noted that we also observe an increase in the generation rate of minority charge carriers after field action. The creation of holes occurs mainly on the reverse branches in the measurements, and their accumulation can be evaluated from the divergence of the curves of p_{sq}. However, in this case, the values of p_{sq} must be compared for identical band bendings in the semiconductor. Therefore, in the inset in Fig. 4, we show the dependences $p_{sq}(v_s)$ for the forward and reverse branches obtained by measurements in the states before and immediately after the stress of the insulator. It can be seen that the required concentration of minority charge carriers are reached earlier in the state immediately after the stress.

In summary, we formulate the main conclusion of the study. The action of a high, but pre-breakdown electric field on an ultrathin insulating layer brings about the formation of additional localized interface electron states at a level separated from the bottom of the silicon conduction band by 0.14 eV. Since the recharging of newly formed centers with increasing field stress knowingly provides the accumulation of excess charge with the concentration 8×10^{12} cm^{-2} at the silicon–oxide interface, the total number of new localized states can exceed 10^{13} cm^{-2}. Such a large charge near the semiconductor–insulator interface is bound to have a decisive effect on the change in the tunnel current–voltage characteristics of Si–MOS structures after stress.

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[1] N_c is the effective density of states in the conduction band of silicon.

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