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Σ-Δ modulator for HTS ADC based on the ramp-type Josephson junctions.

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ABSTRACT: An all high-T_c modulator for Σ-Δ analog-to-digital converters (ADC) was optimized with parameters determined by a ramp type Josephson junction technology having a critical current spread less than 13% and using four superconducting layers. Equivalent circuit inductances were extracted from layouts with the help of a new multilayer 3D- MLSI software package. The resulting performance of the ADC is analyzed in detail and possible improvements are discussed.

1. INTRODUCTION

Numerous suggestions have been made to implement superconducting analog-to-digital converters (ADC). At the hi-end of that research are oversampling ADCs based on Σ-Δ and Δ modulation techniques (Przybysz et al. (1993) and Semenov et al. (1997)). The first fully operational Δ ADC with on chip RSFQ digital signal processing was successfully fabricated in niobium technology and the demonstrated performance was about 16 Spurious Free Dynamic Range (SFDR) at 5MHz signal bandwidth (Semenov et al (1997)).

High-T_c based ADCs may have advantage to their low-T_c analogs due to at least 10 times higher sampling frequency that is determined by the I_cR_n product of the Josephson junctions. An complicated technology that satisfies all requirements on HTS digital circuit still has to be developed to obtain such performance.

Among the different types of HTS Josephson junction technologies, the ramp type junction technology is one of the most promising due to its natural multilayer structure. It was recently reported by Sonnenberg (1999) and Huang (1999) and that this technology provides critical current spread of less than 13% and hence allows device fabrication using 30-50 Josephson junctions.

In this paper, we evaluate the performance of a Σ-Δ modulator that can be realized in a ramp type Josephson junction fabrication process with four superconducting layers.

2. BASIC CONCEPT

Following the approach of Przybysz et al. (1993), a first-order superconducting Σ-Δ modulator can be constructed as a combination of an *R/L* integrator, a quantizer formed by a balanced comparator *J0*, *J1* (Filippov et al. (1995)), sampling and output pulses conditioners *J3-J5* and *J6-J9* (see Fig. 1). The components are well known and will not be described in detail here.

The performance of the modulator is determined by the speed and accuracy of the quantizer. An independent optimization of the balanced comparator (the same schematic but without the R/L loop) shows that the maximum operational frequency of $0.24f_c$ can be reached under the condition of 30% margins on the circuit parameters is equal. Under the same conditions, we kept the threshold

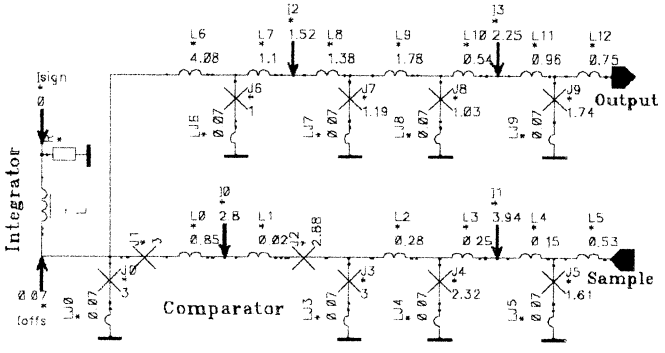

Fig. 1. Equivalent circuit of the Σ-Δ modulator. The parameters are given in units normalized to the minimal critical current (J6).

misplacement as small as possible. The optimization resulted in a minimum threshold misplacement of about $3\%I_c(J0)$. Corresponding optimal working parameters are indicated in the figure.

The R/L pole of the integrator is determined by the useful signal bandwidth and the value of the thermally induced threshold misplacement of the quantizer, ΔI_{thr}. It was shown by Przbysz et al. (1993), that at $\Delta I_{thr}=0.2\Delta$ ($\Delta=\Phi_0/L$) and input signal frequency f twice as large as the integrator pole $R/2\pi L$, the Σ-Δ modulator can have a regular increase in signal to noise ratio (SNR) by *9dB/octave* of oversampling.

The output of the modulator represents the input signal together with its out-of-band components and has to be passed through a digital low-pass filter to attenuate it. Under the limiting condition on the number of Josephson junctions, the decimation filter can be replaced by a counter formed from a T-flip-flop with an SFQ/DC converter proposed by Likharev and Semenov (1991).

3. FABRICATION PROCESS

The HTS ramp junction technology that can be used to fabricate the Σ-Δ ADC fabrication has to satisfy minimal requirements on the circuit topology and inductive parameters. In order to achieve this, the structure has to be integrated over a ground plane; the Josephson junctions have to be formed with a rotating substrate during the etching to achieve their arbitrary orientation and an additional superconducting layer should provide a connection of the two electrodes of the Josephson junctions to the ground plane. A sketch of the process that employs all these features is shown in Fig. 2.

Since the quality of the ramp junctions is very sensitive to the roughness of the films, the four layer structure with ground plane M0, insulator I0, bottom electrode of the Josephson junction M1 and insulator I1 have to be prepared in situ in one technology step. Such a structure was deposited and he measured roughness was about 15nm. All films were grown by pulsed laser deposition at 800°C and 0.2mbar oxygen pressure.

The Josephson junction fabrication process was established independently. Smooth ramps with angles of 25-29° to the substrate were formed in M1/I1 layers using an Ar^+ milling through a hard baked photoresist mask with an etch angle of 45° normal to the rotating substrate. The 25nm thick PBCGO barrier and the upper electrode M2 were then deposited and patterned. The junctions showed RSJ like behavior with $J_c(4.2K)\approx10^4 A/cm^2$, $I_cR_n(4.2K)\approx4mV$ and 1σ spread measured over 27 junctions less than *13%*. A detailed description of the technology process and experimental results can be found in [4].

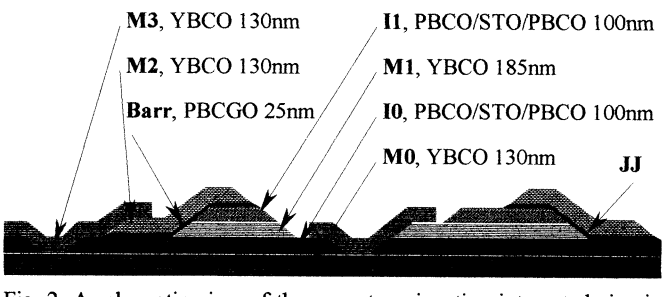

Fig. 2. A schematic view of the ramp type junction integrated circuit. Contacts to ground are made through the M3 electrode.

An additional YBCO layer M3 is going to be used for "via" connection

to the groundplane. The windows in insulators I0, I1 can be opened in one technology step. The etching conditions should be the same as in the ramp preparation to avoid the appearance of the step-edge Josephson junctions in M3 layer. Measurements of the parameters of the Josephson junctions, before and after heating them at the YBCO deposition temperature, indicated that the addition of the fourth superconducting layer to the process costs 20% decrease in the critical current density.

4. CIRCUIT DESIGN

Several circuits were designed for experimental testing: balanced comparator, T-flip-flop, DC/SFQ converter and SFQ/DC converter.

The minimum critical current of Josephson junctions, I_c^{min}, was chosen to give a sufficiently low bit error rate $P=10^{-16}$ *1/bit*. The incorrect switching, with probability P, in pairs of competitive Josephson junctions (balanced comparator) was considered as a major source of error in the circuits. To find the relation between the required value of I_c^{min} and the working temperature T, we can apply the equation for the probability P for a certain value of the measured current I near the threshold I_{thr} (Filippov (1995)):

$$P = 1 - erf(\sqrt{\pi}\frac{I_{thr} - I}{\Delta I_{thr}}), \quad \Delta I_{thr}[\mu A] = 10^3\left(2\pi\frac{2\pi k_B T}{\Phi_0}\right)^{1/2}\left(I_c^{\min}\right)^{1/2}$$

where ΔI_{thr} is the effective threshold uncertainty. When the current I is considerably far from the threshold I_{thr}-I=30%I_c^{min}, the minimal critical current will be given by $I_c^{min}[\mu A]=34T[K]$.

The range of critical current is also limited by the criterion $w \le 4\lambda_J$, where w is the width of the Josephson junction. If the normalized critical currents in the circuit range between I_c^{min} and $2I_c^{min}$, then the temperature dependence of I_c^{min} in ramp type junctions can be expressed by:

$$I_c^{\min} \le 2\lambda_J \frac{h}{\sin(\alpha)} J_c(T) = \left(\frac{\Phi_0 J_c(T)}{2\pi\lambda_L(T)\mu_0}\right)^{1/2} \frac{h}{\sin(\alpha)},$$

where h is the width of the bottom electrode film and α is the ramp angle.

Thus, for the given technological parameters of $J_c(4.2K)=8*10^3 A/cm^2$, $\lambda_L(4.2)=180nm$, $h=184nm$ and $\alpha=25°$, the available range of the critical currents vary from $I_c^{min}=203\mu A$ ($w=6.4\mu m$) to $2I_c^{min}=410\mu A$ ($w=13\mu m$). The estimated working temperature is about $T=7K$, which results in simulation units of voltage, resistance, inductance and frequency of $I_cR_n=3.1mV$, $R_n=15.3\Omega$, $\Phi_0/2\pi I_c=1.62pH$ and $2\pi I_cR_n/\Phi_0=9.47THz$ respectively.

Fig. 3 shows the schematic and the corresponding layout of the most complex part, an SFQ/DC converter. The equivalent scheme inductances were extracted with the help of the 3D-MLSI (3D MultiLayer Superconducting Inductances) program (Khapaev (1999)). This program takes into

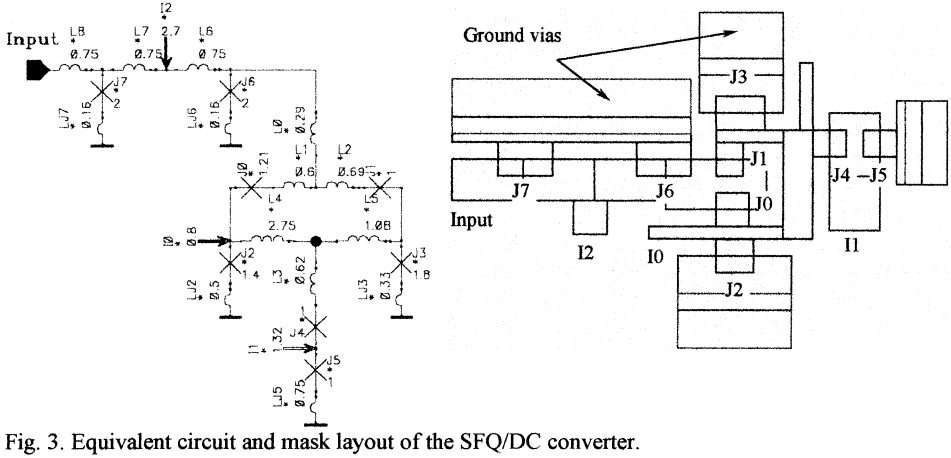

Fig. 3. Equivalent circuit and mask layout of the SFQ/DC converter.

account the 3D distribution of the magnetic field in the structure caused by high values of the London penetration depth compared to the thicknesses of the layers.

We have optimized again the parameters of the circuits using the extracted values of the inductances and the estimated critical currents of the Josephson junctions. As a result, the lowest margin is 19% on the critical current of the junction J4 in SFQ/DC converter with the optimal parameters shown in Figure 3. The variation of the parameters of the balanced comparator (see Table 1) did not affect the margins but it has reduced the sampling frequency to $0.1f_c$ and it has increased the threshold uncertainty to 7%(J0).

Table 1. Optimal parameters for balanced comparator in HTS ramp junction technology

J0=2	J1=2	J2=2	J3=2	J4=2
J5=1	J6=1	J7=1.63	J8=2	J9=2
I0=2.3	I1=2.7	I2=1.54	I3=2.7	L0=0.75
L1=0.42	L2=0.96	L3=1.08	L4=0.9	L5=0.75
L6=3.5	L7=1.08	L8=0.8	L9=1.5	L10=0.75
L11=0.75	L12=0.75	LJ0=0.18	LJ3=0.18	LJ4=0.18
LJ5=0.18	LJ6=0.18	LJ7=0.18	LJ8=0.18	LJ9=0.18

With the estimated working parameters the threshold uncertainty of the quantizer is $\Delta I_{thr}=17.8\mu A$ and it defines the minimum of integrator inductance $L=23pH$. It, in turn, limits the input resistor to $R=8m\Omega$ for $60MHz$ input signal bandwidth. A complete Σ-Δ modulator in our existing technology can not be fabricated as it is hard to achieve the required small value of the resistor in the integrator loop due to the high ($\approx 10^{-5}$-$10^{-6}\Omega cm^2$) contact resistance between YBCO and normal metal (Komissinski (1999)).

5. DISCUSSION

The biggest difficulties in the application of HTS Josephson junctions to RSFQ digital circuits have been high inductances and topology restrictions caused by technology limitations. The four-layer ramp junction technology proposed here could overcome these difficulties.

A quantizer and one stage of the counter with SFQ/DC converter optimized for such a process are expected to operate with minimum 19% margins of the parameters and at a sampling frequency of $f_s=150GHz$. The resulting signal to noise ratio is equal to $SNR=f_s/2f=1250$ for a $60MHz$ input signal bandwidth and this provides 3 bits of extra resolution in comparison to low temperature oversampling ADCs. The working temperature is $7K$ and the level of thermal noise induced errors is $BER=10^{-16}$ $1/bit$.

Improvements in the technology by increasing the critical current density up to $J_c=3*10^5 A/cm^2$ and correspondingly decreasing the junction linear size to $1.2\mu m$ should allow an operational temperature of about $30K$. To overcome the difficulties with a small resistor at the input of the Σ-Δ modulator, an alternative Δ modulator can be considered.

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