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Nanoimprinted lithography high performance in-plane organic diodes

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We have used nanoimprint lithography to fabricate organic in-plane diodes whose design and process are suitable for mass produced by roll to roll production for simple radio frequency circuitry. The diode characteristics are a result of a channel constriction with rectifying ratios up to 3.25×10^4. Above the threshold voltage their behavior is quadratic, and there is a non-quadratic relationship between the threshold voltage and channel width and channel length. The phenomenon is the resultant interaction of the distribution of the localized states and the additional in-plane transverse electric field through the device channel. © *2011 American Institute of Physics*. [doi:10.1063/1.3655369]

The very few flexible electronics on foil[1–3] are produced by batch type production, with multiple processes and hence expensive. Low cost can only be realized by using a combination of roll to roll manufacturing process that integrates a small amount of operations and using a device design that is compatible with a high fabrication throughput.[4] We report such a system an in-plane organic nanodiode whose characteristics are a result of a channel constriction not doping nor using differential work functions of the contact electrodes. Our diodes: have high rectifying ratios, up to 3.25×10^4, are fabricated by nanoimprint lithography in a single step, at a low temperature (190 °C).

To-date planar transistors[5–8] and diodes[9] have been fabricated using conventional lithography techniques, on rigid substrates, grown epitaxially at high temperatures (>600 °C), with III-V or II-VI semiconductors. Planar diodes enables single step lithography and can define OR & AND logic components and ring oscillators. Their asymmetric IV characteristics are similar to that of a conventional diode, but their turn on voltage can be widely tuned by simply increasing the device channel width. In addition planar diodes, since they have lower parasitic capacitance than conventional form diodes, they can operate up to 2.5 THz,[10] the fastest nanodiode to-date. For radio frequency (RF) circuitry switch-off is not required, since in small signal the transistor is operated in the on state and the small RF signals that are amplified are superimposed onto the dc gate source voltage; hence complementary metal–oxide–semiconductors (CMOS) is not necessary and P-type metal–oxide–semiconductors (PMOS) will suffice.

Diodes are fabricated by Nano Imprint Lithography (NIL) the boundary of a narrow channel are defined by means of two L-shaped trenches with gap size ranging from 25 to 150 nm with channel lengths varying from 500 to 2000 nm. A 150 mm wafer spin coated with a negative e-beam resist hydrogen silsesquioxane (HSQ) at 1000 rpm for 20 s yields a thickness of 90 nm. A JEOL 9300FS exposes patterns of in-plane diodes with at a dose of 1365 μC/cm^2 the resist was developed in a tetramethyl ammoniumhydroxide solution TMA238WA for 120 s followed by a rinse in H_2O for 60 s and a hard bake on a hot plate at 200 °C for 120 s. Si wafer was etched to a depth of 197 nm via reactive ion etching with a gas blend of SF_6/O_2. To fit into the hydraulic press the stamp had a protective photoresist spun on, hard baked, and reduced in size by laser ablation before a tapered polish on the edges of the wafer to remove debris. With the removal of the protective resist the final stamp was realize, as shown in Figs. 1(b) and 1(c). The Si stamp was coated with octadecantrichlorosilane (OTS) to form a fluorinated terminated self assembly monolayer (SAM) on the surface. To form the SAM the stamp was cleaned with an O_2 plasma to remove all organic contaminants and form a thin layer of surface oxide and silanol groups on the stamp. Finally the clean stamp was transferred to a dessicator, evacuated, and exposed to OTS at 2 mTorr overnight. Functionalisation of the stamp surface lowers the surface energy compared to the cross-linked poly-4-vinylphenol (PVP) coated substrate thereby facilitating separation of the Si stamp from the PVP after imprinting.

On 100 mm N++ doped Si wafers, 200 nm of SiO_2 was thermally grown. A solution of 10% of PVP and 2% cross linker by weight dissolved in propylene glycol methyl ether actate (PGMEA) was spin coated at 5000 rpm for 60 s and softbaked at 120 °C for 120 s. The spin and soft baked cycle was repeated twice to give a film thickness of 600 nm and wafer. Wafer was baked in a vacuum oven at 150 °C for 3 h to ensure removal of all solvent.

The OTS treated Si stamp and PVP coater wafer was careful mounted in the high pressure hydraulic press located in a class 1000 clean room environment to avoid possible dust contamination. System was heated above the glass transition temperature (T_g) of PVP to 190 °C before a force of 5000 kg was applied for 20 min. Pressure removed and stamp and wafer allowed to return to room temperature before being carefully separated to yield the imprinted PVP. To improve charge injection into the organic semiconductor 5 nm and 30 nm of Ti/Au electrodes were evaporated and

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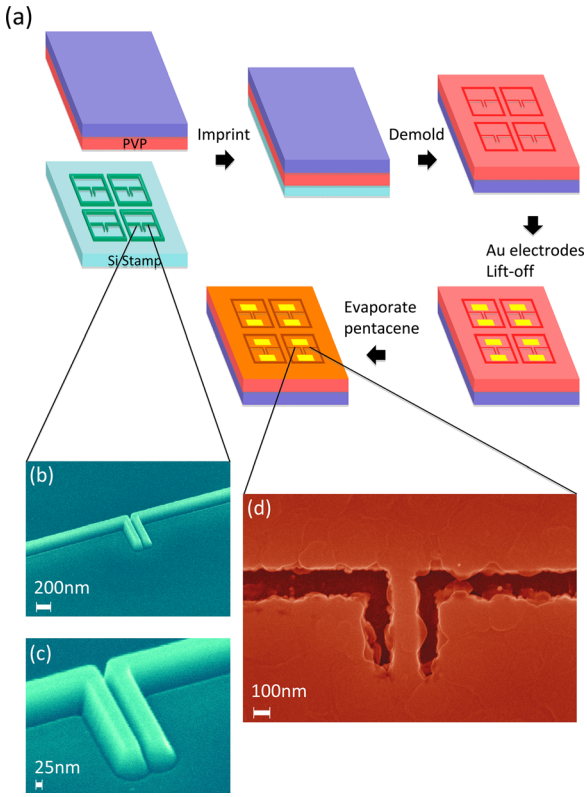

FIG. 1. (Color online) (a) Schematic of process flow for fabricating organic in-plane diodes. (b) SEM image of W = 25 nm, L = 500 nm Si stamp (c) Magnified SEM image of W = 25 nm, L = 500 nm Si stamp (d) SEM image of W = 150 nm, L = 500 nm finalized device.

defined by lift-off via an aligned photo resin mask with respect to the etch trenches.

Prior to evaporation, to induce preferable pentacene growth and improve charge injection, the substrate was exposed for 15 min to UV ozone to remove organic contaminations, and then a SAM of pentflorobenzenethiol (PFBT) was applied by solution immersion to the Au electrodes followed by 2-phenylethyltrichlorosilane (PETS) applied by vapour phase at 60 °C in vacuum. A 30 nm film of pentacene was evaporated on the wafer under UHV ($P = 4 \times 10^{-8}$ Torr), with $T_{substrate} = 68$ °C and a deposition rate of ~0.25 Å s^{-1}. A calibrated quartz crystal monitor held at 297 K was used to measure the deposition rate and film thickness, with finalised device shown in Fig. 1(d). Wafers were transferred under a nitrogen atmosphere to a darkened nitrogen glove box [$H_2O < 0.1$ ppm and $O_2 < 0.1$ ppm] where the electrical measurements were performed. Device IV characteristics were measured on a probe station with data taken by a HP semiconductor analyzer. After all electrical measurements have been performed, the devices channel widths and lengths were measured using a SiN high resolution tip and vecco nanoscope atomic force microscope.

Before devices were measured it was verified that all devices were indeed electrically isolated with respect to each other, applying a bias of 10 volts a leakage current between 20 nA to 0.09 nA was observed. Figure 2 plots I-V characteristics of the pentacene in-plane diodes at room temperature, rectifying behavior is seen in all measured devices. Undesirable leakage varies from 20 to 0.09 nA; also, there is a wafer to wafer variation, which indicate that the process and hence

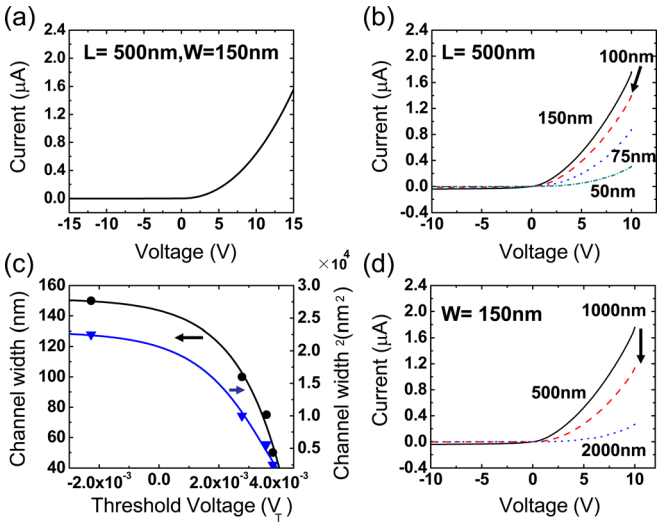

FIG. 2. (Color online) Pentacene in-plane diode: (a) I-V characteristics, (b) I-V characteristics with different channel widths, (c) threshold voltage vs. channel width (•) and W^2 (▼), (d) I-V characteristics of different channel lengths.

device performance may be further optimized. The W = 150 nm device had the best performance; in forward bias a current of 1.56 μA is seen at V = +15 V bias, with a rectification ratio of 3.25×10^4 at ±15 V as shown in Fig. 2(a). Various channel widths, W = 50-150 nm for the same channel length of L = 500 nm are plotted in Fig. 2(b) a second W = 150 nm device has a rectification ratio of 780 at ±10 V. Current above V_T with forward biasing is proportional to V^2; at voltages well above V_T the current is linear with the increase gap width. Threshold voltage V_T [Fig. 2(c)] is plotted against the channel width W and W^2 (right-hand axis), data can be fitted with W = A + Bexp (−V/C), the depletion width when $V_T = 0$ V is ~73 nm (depletion width ≈ channel width/2). Devices with W = 150 nm, for channel lengths of 500, 1000, and 2000 nm are plotted similarly; at voltages, well above V_T current is linear with L and V_T is also exponential with respect to L.

Previous planar diodes[9] III-V hetrostructure semiconductors, ($In_{0.75}Ga_{0.25}As/InP$ or $In_{0.53}Ga_{0.47}As/In_{0.53}Al_{0.47}As$) operate in inversion and depletion modes. Their asymmetric IV is a function channel constriction and the bias applied across it. Appling a bias modifies the depletion within the channel, such that for a given channel width the channel will be fully depleted and pinched off so no current flows.

In contrast, an organic in-plane diode will operate in accumulation and depletion mode, we propose the organic in-plane system work as thus:

Appling a bias creates a potential gradient along the channel, with a positive bias $V > V_T$ between the right and left Au contacts, the holes which are majority charge carriers in pentacene accumulate in the channel current flows and varies with V^2, whose slope depends on the RC of the diode, the depletion capacitance C and the channel resistance of the pentacene R (>6.2 MΩ).

When a negative bias is applied, depletion within the channel starts, the voltage gradient along the channel length causes a depletion gradient along the channel, such that at $V > V_T$, the channel is wholly pinched off, with only the leakage current contributing.

It is similar to an organic Schottky contact[11–13] but our device does not have a metal-semiconductor interface. The latter devices are of a sandwich or bottom gate transistor design which also display diode like characteristics and a non-quadratic variation of the threshold voltage verses depletion width, this variation originates from the distribution of localized states.

The depletion width in a Scottky contact with a crystalline semiconductor and metal can be analytically determined via Poisson's equation, for a uniformly doped semiconductor, the electrical field is linear with distance from the junction and a quadratic potential in the depletion region, hence the depletion width W_{dep}^2 is proportional to bias voltage V.

However, this does not apply to organic semiconductors since the depletion widths cannot be analytically determined, as the net charge density in the depletion region is the summation of the density of the ionized dopents and the density of trapped charges in the localized state.[14] Since the density of the trapped charges is not constant in the depletion region and it changes with the bias voltage Poisson's equation has to be solved numerical to obtain the depletion width.

The effective density of states (DOS) in an organic film is low (in Si the DOS conduction band at 300 K $3.22 \times 10^{19}\,cm^{-3}$) and sensitive to molecular ordering, with static and dynamic disorder in position and orientation affecting molecular energies through electrostatic and static interactions. Hence diode behavior was not expected however since rectification is observed this implies a high density of states within the channel.

Trapping/detrapping,[15–17] a field-activated mobility,[18] are possible but a more likely mechanism is charging of grain boundaries in one or two dimensions.[19,20] Kelvin probe force microscopy[21] shows an additional peak in the main DOS distribution at interfaces between regions of different surface potential, the transverse electric field gradient along the channel due to in-plane device geometry may have a role in enhancing this mechanism.

Limited studies of pentacene nanometer-sized channel devices[22–24] are of bottom-gate architectures and the pinch-off regime was not investigated.

The resultant threshold voltage and around the pinch-off regime will be very sensitive to the charge accumulation which is closely related to the electric field profile. Further work is needed, scanning Kelvin probe force microscopy to probe the DOS and charge carrier accumulation and the on set of conduction and finally a full model with a self-consistent calculation to include the three dimensional potential profile would be insightful.

We have demonstrated nanoimprinted organic in-plane diodes whose design and process are suitable for mass produced by roll to roll production for simple RF circuitry. Diode characteristics are a result of a channel constriction with rectifying ratios up to 3.25×10^4. Above the threshold voltage their behavior is quadratic, and there is a non-quadratic relationship between the threshold voltage and channel width and channel length. Behaviour is the resultant interaction of the distribution of the localized states and the additional in-plane transverse electric field through the device channel.

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