High-Harmonic Phase Detector based on SIS junction

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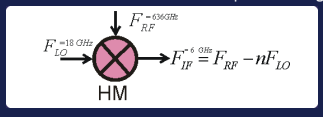
Abstract

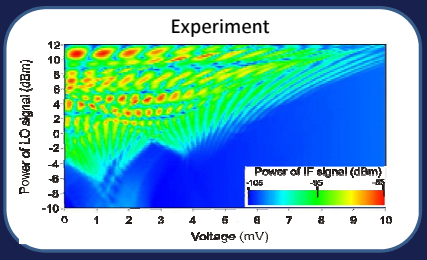
A novel superconducting element, High-Harmonic Phase Detector (HPD), intended for phase-locking of a Flux Flow Oscillator (FFO) in a superconducting integrated receiver (SIR) has been proposed and experimentally tested. According to our concept a high harmonic of a reference local oscillator (LO) signal (frequency of about 20 GHz) produced in the SIS junction is mixed by the same junction with FFO signal (frequency of order 600 GHz); the HPD output is applied directly to the FFO control line to correct its phase and frequency. To realize efficient FFO phase-locking the HPD output signal is maximized by tuning the HPD bias voltage, the RF power, the LO power and frequency (harmonic number). Calculated 3D dependences of the HPD output signal power versus bias voltage and LO power correspond well to experimental measurements.

To demonstrate that the FFO signal has been phase-locked by the HPD we used an additional SIS-mixer with receiving antenna and monitored its intermediate frequency (IF) output. The regulation bandwidth (BW) of the phase-locking loop (PLL) system based on the HPD as wide as 70 MHz has been measured experimentally; that value several times exceeds the BW of regular PLL systems used for cryogenic oscillators. New PLL system based on HPD synchronizes up to 92% of the emitted FFO power (this parameter is called the spectral ratio, SR) for free running FFO line as wide as 12 MHz The HPD PLL system is simple and compact, therefore it is very promising for future SIR applications, especially for building multi-pixel SIR arrays and for phase-locking of the THz range FFO.

Theoretical and experimental study of Harmonic Mixer based on SIS junction

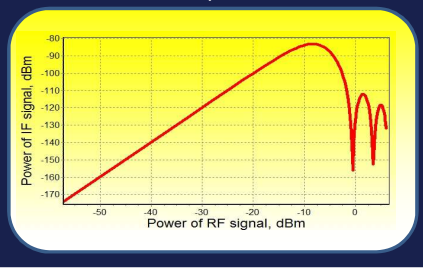
When two signals of frequencies f_1 and f_2 are applied to the SIS junction, the signals on every combination frequency $f = nf_1 \pm mf_2, \forall n,m \in N$ appear. Let us consider the smallest frequency signal, i.e. $I_{IF} = \alpha_k \cos(2\pi(f_1+kf_2)t+\varphi_{0k})$. Thus, the harmonic mixer operates as a high-harmonic phase detector and could be used for phase locking loop system. It is crucial to achieve a high-power output signal of the harmonic mixer based on the SIS to realize efficient FFO phase-locking. The theoretical study of the HM power characteristics has been performed. The results of numerical calculations coincide well with experimental measurements.

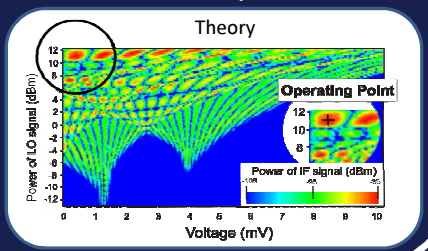




When two signals of frequencies 635 GHz and 18 GHz (its 35-th harmonic is used) are applied to the HM based on the Nb-AlOx-Nb SIS junction (size 1x1 um2 with Rn of about 25 Ohm), the maximal output power is about -90 dBm.

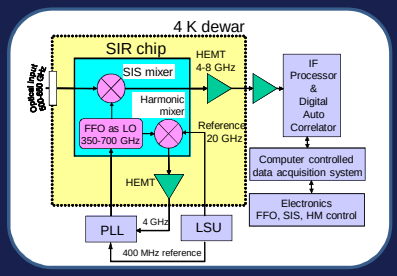
Calculated power characteristics of Harmonic Mixer based on SIS junction





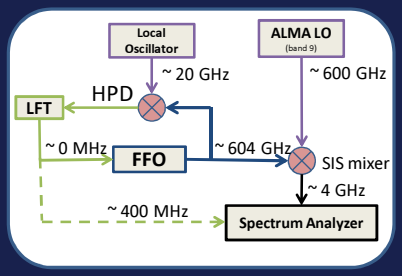
New approach for FFO Phase-Locking

Block Diagram of the Superconducting Integrated Receiver



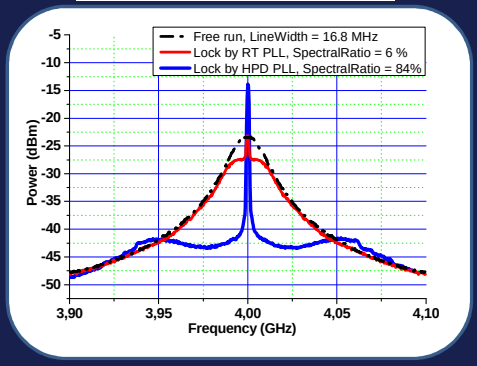
In the SIR the FFO is phase-locked by a conventional room temperature (RT) PLL system. The traditional PLL is a semiconductor-based device designed for 300 K, and it cannot be placed directly in the cryostat. Due to the total delay of about of 17 ns in connection cables, the BW for RT PLL is limited by 12 MHz .

Concept of FFO synchronization by Harmonic Phase Detector



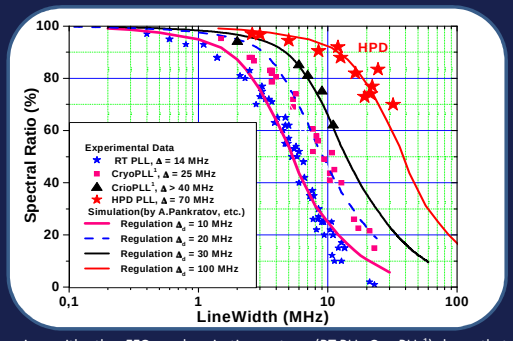
We proposed to use harmonic mixer for phase-locking of the FFO to an external reference by applying the HPD output directly to the FFO control line. It allows us to place all the PLL elements close to the FFO. So the delay in the loop decreases, and as result the bandwidth can be increased up to 100 MHz .

FFO Spectrum locked by HPD



The HPD PLL has been experimentally implemented. The results of the FFO spectra measurements prove the HPD PLL concept and demonstrate its efficiency. The regulation bandwidth of HPD PLL system of about 70 MHz has been measured. For the FFO line as wide as 17 MHz the HPD PLL phase locked up to 85% of emitted by FFO power, which is incomparably more than 6% synchronized by the traditional RT PLL for the same FFO line.

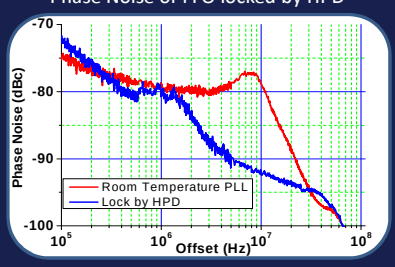
Comparison HPD PLL with analogues



Comparison with other FFO synchronization systems (RT PLL, CryoPLL [1]) shows that proposed approach has definite advantage over the conventional PLLs. High efficiency, small size, low power consumption and simplicity make the HPD attractive for future applications, such as ultra wide baseline interferometry and development of receiver array.

[1] Detailed information about CryoPLL could be found in the article *A.V. Khudchenko et.al. "Cryogenic Phase Locking Loop System for Superconducting Integrated Receiver", SuST, 22, 085012, 2009.*

Phase Noise of FFO locked by HPD



Characteristics of some PLL systems

	RT PLL	CryoPLL[1]	HPD PLL
Delay, ns	17	9	< 4
BandWidth, MHz	14	25	70
LW for SR > 90 %, MHz	1,6	3,2	12
SR for LW = 22 MHz, %	2	15	77

Summary

✓ The novel application of the SIS junction – the Cryogenic High-Harmonic Phase Detector (HPD) has been proposed.

✓ The theoretical and experimental studies of the HM are performed; measured results are in a good qualitative and quantitative agreement with numerical calculations.

✓ The concept of the HPD is experimentally realized; regulation bandwidth of the HPD PLL as wide as 70 MHz has been demonstrated.

✓ High efficient FFO phase locking (SR > 90% for the FFO linewidth of 12 MHz) and considerable decrease of the FFO phase noise have been achieved.

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