Chapter 11
Cryogenic Phase-Locking Loop System Based on SIS Tunnel Junction

A.V. Khudchenko, V.P. Koshelets, and K.V. Kalashnikov

Abstract An ultra-wideband cryogenic phase-locking loop (CPLL) system is a new cryogenic device. The CPLL is intended for phase-locking of a Flux-Flow Oscillator (FFO) in a Superconducting Integrated Receiver (SIR) but can be used for any cryogenic terahertz oscillator. The key element of the CPLL is Cryogenic Phase Detector (CPD), a recently proposed new superconducting element. The CPD is an innovative implementation of superconductor–insulator–superconductor (SIS) tunnel junction. All components of the CPLL reside inside a cryostat at 4.2 K, with the loop length of about 50 cm and the total loop delay 5.5 ns. Such a small delay results in CPLL synchronization bandwidth as wide as 40 MHz and allows phase-locking of more than 60% of the power emitted by the FFO even for FFO linewidth of about 10 MHz. This percentage of phase-locked power three times exceeds that achieved with conventional room-temperature PLLs. Such an improvement enables reducing the FFO phase noise and extending the SIR operation range.

Another new approach to the FFO phase-locking has been proposed and experimentally verified. The FFO has been synchronized by a cryogenic harmonic phase detector (CHPD) based on the SIS junction. The CHPD operates simultaneously as the harmonic mixer (HM) and phase detector. We have studied the HM based on the SIS junction theoretically; in particular we calculated 3D dependences of the HM output signal power versus the bias voltage and the LO power. Results of the calculations have been compared with experimental measurements. Good qualitative

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and quantitative correspondence has been achieved. The FFO phase-locking by the CHPD has been demonstrated. Such a PLL system is expected to be extra wideband. This concept is very promising for building of the multi-pixel SIR array.

11.1 Introduction

A cryogenic phase-locking loop (CPLL) system is primarily intended for phase stabilization of a Local Oscillator (LO) of a Superconducting Integrated Receiver (SIR) [1, 2]. The SIR circuit embodied on a chip (size of $4 \times 4 \times 0.5$ mm) comprises a low-noise superconductor–insulator–superconductor (SIS) mixer with quasioptical planar antenna, a superconducting Flux-Flow Oscillator (FFO) acting as a tunable LO in the frequency range 400–700 GHz and a second SIS harmonic mixer (HM) to phase-lock the FFO.

The FFO emission spectrum was found to be the Lorentz line [3,4] at frequencies up to 750 GHz. Such line shape indicates that the free-running ("natural") FFO linewidth is determined by the wideband noise, that is thermal fluctuations and the shot noise. This is contrary to many traditional microwave oscillators (e.g., backward-wave and Gunn oscillators), where the "natural" linewidth is rather narrow and is broadened primarily by external fluctuations. In fact, the FFO linewidth may be up to 10 MHz. Therefore, for higher spectral resolution, FFO frequency should be stabilized with a wideband phase-locking loop (PLL) system. The wider is PLL synchronization bandwidth (BW), the larger part of the FFO power can be phase-locked (PL), resulting in lower phase noise.

The ratio of the phase-locked power to the total power emitted by the oscillator is called a "spectral ratio" (SR). Actually, the SR is determined from a measured LO spectrum as a ratio of the phase-locked power of the carrier to the total emitted power comprising the carrier and the intrinsic phase noise power generated by LO [4]. So, the SR would be 100% for an ideal LO with a delta-shaped spectrum and zero phase noise level. Usually, the noise power is embedded in the bandwidth 100 MHz. It should be noted that measured phase noise includes a contribution of the IF amplifier, and we do not subtract this level in SR calculations (so the actual SR is even a little higher). The error introduced due to IF amplifier noise is about 1–3%. A specially designed semiconductor room temperature PLL (RT PLL) with the BW of about 12 MHz is used for the FFO phase locking. The RT PLL provides SR value of about 50% for the 5 MHz-wide FFO emission line.

There are several reasons to extend BW of the PLL system much beyond the present 12 MHz. The first one is that the FFO linewidth exceeds 10 MHz at the voltages exceeding one-third of the FFO gap voltage, where the Josephson self-coupling effect drastically modifies FFO I–V curves increasing differential resistance and internal damping [5, 6]. In case of such a wide line, an essential part of the emitted FFO power cannot be phase-locked with the RT PLL (the SR is as low as 20–25%). The second reason is that FFOs based on NbN or NbTiN films are the most attractive for future SIR applications at frequencies of about 1 THz. The linewidth of such FFOs can considerably exceed 10 MHz due to higher surface

losses. In this situation, the PLL's bandwidth has to be as large as 50 MHz (to reach at least 50% of the SR value required for most applications). The third reason is that using SIR for interferometery applications requires an LO with extremely high phase stability. For example, for the ALMA project (interferometer in Chile with baseline up to 15 km) the LO rms phase noise should be considerably less than 75 fs (the value of rms atmospheric fluctuation at interferometer site) [7]. The required value of the SR for this rms phase noise level at frequency of about 600 GHz is more than 95%. To provide such a high SR value even for the FFO with relatively narrow linewidth of 2 MHz, the PLL should have BW of about 50 MHz.

The BW is determined by the group delay τ in the loop [8, 9]. It should be emphasized that the noise of RT PLL elements is low enough as compared to the noise of IF amplifier, and it does not affect phase-locking efficiency. For RT PLL, the BW is limited to 12 MHz due to the total delay of about 15 ns (including 5 ns contribution from the PLL filters and semiconductor electronics and 10 ns from the 2 m-long cables connecting the RT PLL electronics with cryogenic FFO). The minimal cabling length is restricted by the size of a cryostat and cannot be essentially reduced without increasing the heat flux into the cryogenic space. Note that the traditional PLL is a semiconductor-based device designed for 300 K, and it cannot be placed directly into the cryostat.

To improve spectral characteristics of the FFO and to overcome the limitation of the RT PLL, we propose the CPLL system based on a Cryogenic Phase Detector (CPD) [8–10]. All elements of the CPLL can be located very close to the FFO inside the cryostat to avoid any temperature gradients between FFO and phase detector and to minimize the loop length. Negligible CPD delay and small group delays in the short loop enable an ultra-wide BW.

11.2 CPD Properties

The CPD is a key element of the CPLL. It is new cryo-electronic device based on micron-sized SIS tunnel junction with a tunnel barrier of about 1–2 nm. The junction has current density 5–10 kA/cm^2, and the gap voltage V_g is 2.8 mV for Nb–AlO_x–Nb circuits.

Synchronization systems theory shows that any mixer can operate as a phase detector [11]. The SIS junction is a well-known mixer element due to its nonlinear properties [12, 13] and can be utilized as a CPD for the CPLL.

There are several advantages of the SIS implementation for the FFO phase-locking. First of all, the SIS junction has a power consumption of about 10^{-6} W that is much smaller than 10^{-3} W for semiconductor diode phase detectors, and second, both the SIS and the FFO operate at temperature 4.2 K. These peculiarities allow place the CPD and the FFO close to each other, and even integrate them on the same chip. Such a PLL system will be very compact and extra wideband.

The output signal of the phase detector with a sinusoidal response is:

$$\varepsilon(t) = mA_1A_2 \sin\varphi(t) = K_{\mathrm{PD}} \sin\varphi(t),$$

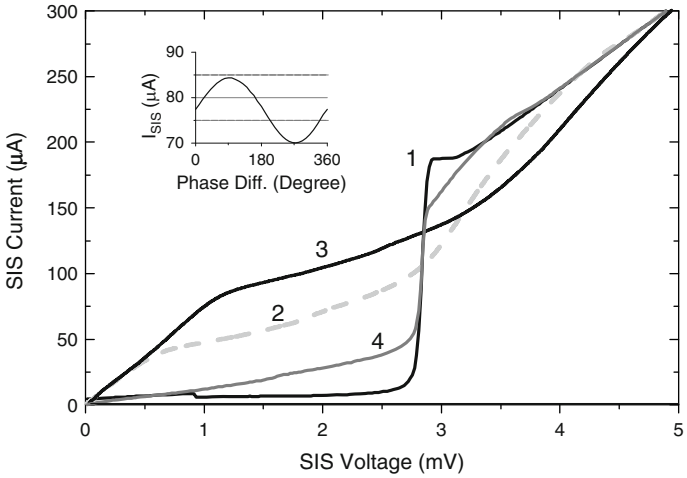

Fig. 11.1 *I–V* curves of the SIS junction measured at various settings of the microwave signals (frequency 5 GHz): curve "1" – autonomous; "2" – pumped by one microwave signal; "3" – pumped by two in-phase microwave signals; "4" – pumped by two anti-phase microwave signals; PSynth1 = 0.3 μW, PSynt2 = 0.1 μW. *Inset* shows a sinusoidal dependence of the SIS current vs phase difference between the signals. Junction aria is about 2 μ^2 with R_nS product about 30 $\Omega\mu^2$

where $\varphi(t)$ is a phase difference between input signals, K_{PD} – a phase detector gain factor, which is equal to the maximum amplitude of the output signal; m – a mixer efficiency, A_1 and A_2 – input signals amplitudes. The phase characteristic of an SIS-mixer (it can be nonsinusoidal), frequency and amplitude properties of output signal and optimal amplitudes and frequencies of input signals must be determined. In this case, such a junction will be specified as a phase detector.

A principle of CPD operation can be demonstrated by the tunnel junction *I–V* curves. A typical autonomous *I–V* curve of the SIS junction is shown in Fig. 11.1 (curve 1); the curve 2 corresponds to the *I–V* curves of the SIS pumped by a microwave signal [8]. Two microwave signals applied in phase give a higher power and a higher pumping level (curve 3), while antiphase results in the lower pumping level (curve 4). The difference between curve 3 and curve 4 corresponds to the phase response amplitude. It is important that this difference is rather large in the wide range of the CPD bias voltages.

The CPD is a unique phase detector due to nonlinearity of the SIS junction [12]. Although the frequency of the synthesizer for curves 2–4 is a few gighertz (corresponding voltage is rather low compared to the smearing of the junction superconducting gap), the shape of the pumped CPD *I–V* curve looks like a result of irradiation by a high frequency signal. Apparently, a certain number of higher order harmonics of the applied signal are excited in the SIS junction due to its nonlinearity; these harmonics effectively pump the tunnel junction. We have compared experimental *I–V* curves and dependence of the CPD pump current as a function of power of the applied signal with the simulated ones. The calculations

were performed on the basis of the Tien–Gordon formula for photon-assisted tunneling (see, e.g. [12]). The best fit to the experimental results was found for frequency of applied signal in the range of 80–100 GHz; at that point, the shape of experimental curves qualitatively resembles the theoretical ones for synthesizer frequency in the range of 0.2–20 GHz [9].

11.2.1 Phase Characteristics

It was shown [8] that dependence of the CPD output versus phase difference between the two input signals can be sinusoidal for the CPD under the proper experimental conditions (see inset in Fig. 11.1). The phase response shape is close to sinusoidal if its amplitude is less than 0.1 I_g (I_g is a current jump at the gap voltage). If the amplitude becomes larger, the response shape changes. Small shape deviations are not critical for operation of the PLL system because it works on the slope part of the phase characteristic, i.e. at $\varphi(t) << 1$. For the nonsinusoidal response, the main parameters are the derivative $d\varepsilon(t)/d\varphi(t)$ (that gives the slope K_{PD}) and the amplitude of the linear section of the phase response (these two parameters are equal to the K_{PD} for sinusoidal signal). However when the phase response amplitude is very high and even approaches to I_g, the response shape is usually deformed so strongly that the PLL system works unstable.

11.2.2 Frequency Characteristics

The capacitance of the used SIS junctions is about 0.1 pF. Due to such a small capacitance, the imaginary part of the junction impedance is very large at low frequencies until the value of order 1 GHz. Therefore, the CPD response amplitude remains flat in this range that was confirmed experimentally for frequencies up to 750 MHz [8]. This magnitude essentially exceeds 100 MHz required for the CPLL operation.

The CPD input signal frequency can be ranged from 0.2 MHz to 20 GHz due to nonlinear SIS properties described above. In this range, the operation frequency of the CPLL can be chosen. Actually, the CPLL operation frequency has the upper limit that is restricted only by working frequency of cryogenic HEMT amplifier (value of order 10 GHz). And the lower limit about 0.4 GHz is determined as a magnitude that should be considerably larger than the CPLL output bandwidth BW = 30–50 MHz.

11.2.3 Amplitude Properties

The CPD amplitude properties can be described by the dependence of the output signal versus input signal amplitudes and bias voltage of the SIS junction. From such a dependence, the maximum output signal and optimal input signal amplitudes can be found.

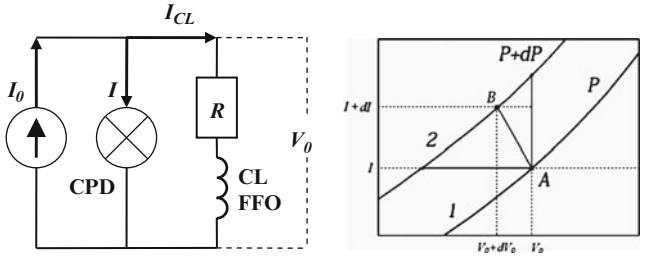

Fig. 11.2 Diagram of the CPD – FFO connection through the resistor R (*left figure*). Part of the CPD I–V curves (*right figure*) in large scale at the voltage $V_0 < V_g$

The CPD of the CPLL is connected to the FFO control line (CL FFO) to tune the FFO frequency [4]. The simplified diagram of the CPD–FFO interface is shown in Fig. 11.2 (left). This equivalent circuit is certainly valid at frequencies of interest 0–100 MHz. The current source generates I_0 and a part of it I splits to the CPD. The CPD voltage V_0 can be expressed in terms of load R and current I by Ohm's law $I_0 = I + V_0/R$.

The tunneling current of the junction changes with increasing of the applied microwave power P (Fig. 11.2 right curves 1 and 2). For the power variation $\mathrm{d}P$, the CPD biasing point goes along the load line $(1/R)$ from point A to point B. The changing of the CPD voltage $\mathrm{d}V_0$ is given by the relation:

$$\mathrm{d}V_0 = -\frac{r_\mathrm{d} R}{r_\mathrm{d} + R}\frac{\partial I}{\partial P}\mathrm{d}P,$$

where r_d is a CPD differential resistance, $\partial I/\partial P$ is a partial derivative (can be calculated from the dependence $I(P)$ measured at the fixed CPD voltage). The maximal available value of the derivative $\partial I/\partial P$ rises with enhancing of the current jump at gap voltage I_g, that is with increasing of the tunnel junction area.

The combined power of two microwave signals of power P_1 and P_2 applied to the junction with a phase difference φ is: $P(\varphi) = P_1 + P_2 + 2\sqrt{P_1 P_2}\cos\varphi$. In PLL system, one of these two signals is generated by local oscillator (LO) and the second one by a reference oscillator. Then the LO is phase-locked the phase difference φ is close to $\pi/2$ and the deviation is small $(\varphi(t) - \pi/2) << 1$, for the CPD we have:

$$\mathrm{d}V_0 = -2\frac{r_\mathrm{d} R}{r_\mathrm{d} + R}\frac{\partial I}{\partial P}\sqrt{P_1 P_2}\mathrm{d}\varphi,$$

here $P = P_1 + P_2$. The r_d and $\partial I/\partial P$ are experimentally measured; the optimal R is of about 10 Ω. The derivative $\partial I/\partial P$ is a function of powers P_1 and P_2 and bias voltage V_0. The detailed analysis of this formula and experimental results show that output signal amplitude can achieve the value of about 0.2 V_g at the bias voltage 0.55 V_g. For the Nb–AlO_x–Nb SIS junction, which I–V curves are shown in the Fig. 11.1, the maximum output signal riches −50 dBm. The dependence of the CPD

maximum output versus V_g is rather flat and stay in 3 dB range at the interval 0.25–0.8 V_g. For the optimal value of the input signals, the induced pumping current of the SIS junction is of about 0.3 I_g.

The contribution to the current I_{CL} from the CPD is determined by the dV_0/R value. Thereby, the phase deviation $d\varphi$ leads to the variation of the FFO frequency df_{FFO}:

$$df_{FFO} = k\,dV_{FFO} = k\frac{dV_0}{R}Rd_{CLFFO} = -kRd_{CL\_FFO}\frac{r_d}{r_d + R}\frac{\partial I}{\partial P}\sqrt{P_1 P_2}d\varphi,$$

here $k = 483.6\,\text{MHz}/\mu\text{V}$ is the Josephson constant and $Rd_{CL\ FFO} = dV_{FFO}/I_{CL}$ is the FFO differential resistance by I_{CL} (typically, about 0.01 Ω).

This formula describes the efficiency of the CPD–FFO coupling; it has been experimentally verified with a good accuracy [9, 14], and used for design of the CPLL. An important result is that the value of df_{FFO} is found to be linearly proportional to the derivative $\partial I/\partial P$, magnitude $Rd_{CL\ FFO}$, amplitudes of the microwave signals, and is determined by the r_d and the R.

The coefficient $K = df_{FFO}/d\varphi$ is the open loop gain in the CPLL system [11,15]. It can be adjusted by variation of the powers P_1 and P_2 to achieve the optimal feedback in the loop providing the maximum SR in the FFO spectra. For the Nb–AlO_x–Nb SIS junction presented in Fig. 11.1, the coefficient K achieves the value 250 MHz/rad at $R = 10\,\Omega$ and $Rd_{CL\,FFO} = 0.01\,\Omega$.

The K also shows the maximum frequency deviation of the FFO, which can be tuned by CPD, that is the holding range of the CPLL system that is an upper limit of the BW. It means that the BW of the PLL system based on the CPD connected directly to the FFO (without any DC amplifier between) can reach the value of about 250 MHz.

11.3 CPLL System: Description and Experimental Results

Several experimental embodiments of the CPLL systems with various operation frequencies and various loop lengths have been developed and tested [8–10, 16]. A flowchart of the latest design is shown in Fig. 11.3. The FFO emission at the frequency of the order of 600 GHz is downconverted by the HM to the frequency 4 GHz and amplified by two HEMT-amplifiers, HEMT 1 and HEMT 2. This signal is compared with the external reference signal by the CPD and the resulting output error signal (proportional to the phase difference) is applied to the FFO to control its frequency. A certain fraction of the microwave power after HEMT 1 is tapped by the directional coupler to the spectrum analyzer. A filter between the CPD and the FFO comprises a rejecter filter to suppress signals close to the reference frequency and an integrating loop filter for locking and holding of the FFO frequency. The integrating loop filter significantly increases stability of the CPLL system. It also considerable decreases a phase noise of the phase-locked FFO near the carrier at frequencies

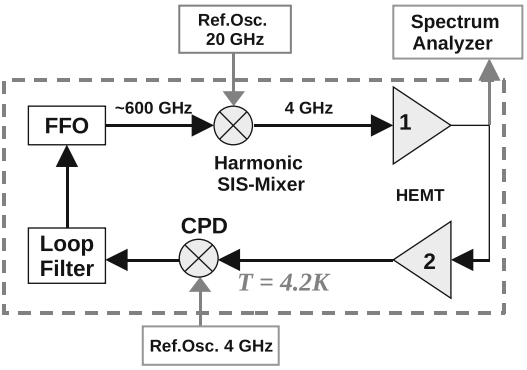

Fig. 11.3 Flow chart of the CPLL for FFO phase locking

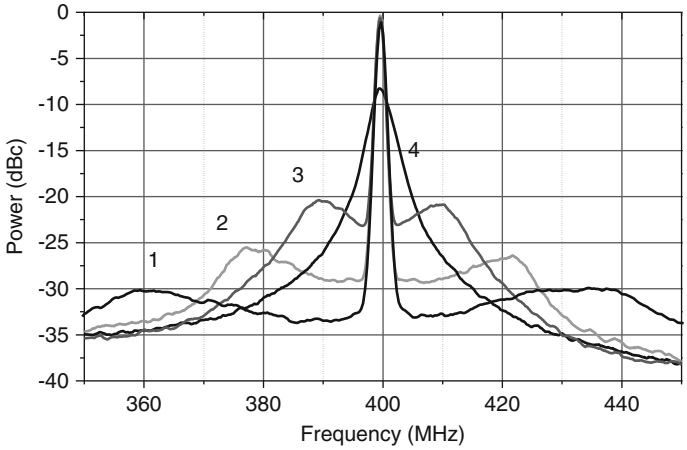

Fig. 11.4 Downconverted spectra of the FFO operating at 600 GHz: curve "1" – Free running, linewidth 2 MHz; "2" – phase-locked with CPLL, BW 40 MHz (SR = 93.5%); "3" – phase-locked with CPLL, BW 25 MHz (SR = 90.5%); "4" – phase-locked with RT PLL, BW 12 MHz (SR = 82%)

offset less 100 kHz. The essential moment is that the filters are based on a passive elements operating at 4.2 K and can be placed close to the FFO and the CPD [16].

In the latest design, the loop length has been reduced down to 50 cm, which corresponds to delay 2.5 ns. The operating frequency for this system was chosen 4 GHz. For such a frequency, a band-stop filter (between CPD and FFO) with delay less than 0.5 ns has been developed. The reduction of the loop delay due to the described modifications results in increasing of the BW up to 40 MHz (see Fig. 11.4, curve 2).

In Fig. 11.4, downconverted spectra of the FFO phase-locked by different PLL systems are presented (spectrum of the free-running FFO is also shown for comparison). It should be noted that all phase-locked spectra have typical shape consisting of a central peak containing locked power, and phase noise shoulders on

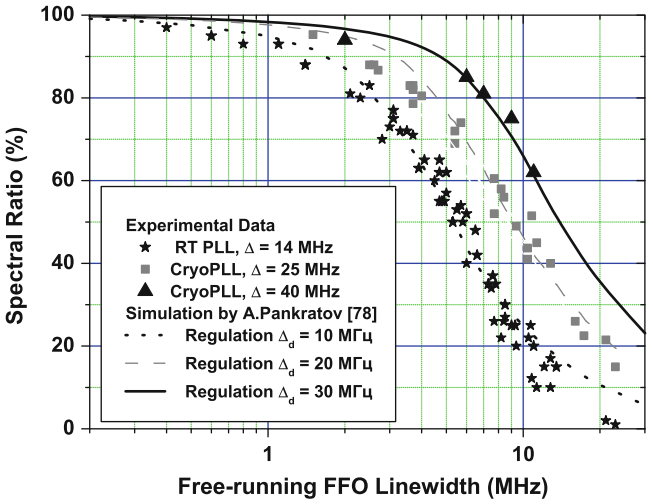

Fig. 11.5 SR vs FFO linewidth for PLL systems with various synchronization bandwidths

sides of the peak. For example, the tops of shoulders for the CPLL with BW 40 MHz are located at offsets 35–40 MHz from the carrier (curve 2 on the Fig. 11.4). At these frequencies, phase of the return signal is shifted by π due to the delay in the loop. So instead of noise suppression, the increasing of the phase noise occurs in the PLL system; position of these shoulders allows estimation of the PLL synchronization BW. These shoulders rise and become sharp with increasing of the PLL loop gain. The optimal PLL gain for any given PLL system is achieved for the shoulders about 3dB higher than phase noise near the carrier. In this case, the maximum SR and signal-to-noise ratio is reached.

From Fig. 11.4 one can see that increasing of the PLL BW leads to expansion of the frequency range, where the phase noise of the PL FFO is lower than the level for the free-running FFO. The reason is that the wider BW of the CPLL enables us using higher loop gain bringing essential reduction of phase noise in the entire regulation bandwidth (frequency of unity gain is shifted to the right) without considerable increase of the phase noise in the shoulders. For the FFO linewidth of 2 MHz, the CPLL is capable of phase-locking of 93.5% power, as compared to 82% for the RT PLL (Fig. 11.4). For the FFO linewidth of 7 MHz, the new CPLL yields SR = 81% instead of 41% for the RT PLL. Even higher gain was obtained at a broader linewidth of 11 MHz for a free-running FFO: SR = 63% in case of CPLL against 23% for RT PLL.

Summary of the obtained results is presented in Fig. 11.5. Experimental data for the RT PLL with the BW of 12 MHz are shown by asterisks, for the CPLL with BW 25 MHz – by squares, and triangles show results for the described above CPLL with BW of 40 MHz. Lines show results of numerical simulations [17] to fit the experiment. The "regulation BW" of 10 MHz in simulations roughly corresponds to the synchronization bandwidth "BW" = 12 MHz in experiment. Data for the

described CPLL are shown as a solid line (effective regulation BW of 30 MHz in simulations); these data show the advantage of BW broadening and prospects for future improvement. There is an easy way to estimate the effect form PLL BW widening: the SR for an FFO with a specific free-running line phase-locked by PLL with a specific BW is the same as SR for a double-width FFO free-running line phase-locked by the PLL with double-width BW (it works like a scale effect). Experimental data analysis demonstrates also that the relative fraction of the phase noise (1 – SR) falls linearly with BW increasing at SR > 50%.

It should be noted that the overall group delay for the described CPLL is estimated as 3 ns, but both BW and SR measurements indicate the delay of about 5.5 ns. It means that the additional delay of about 2.5 ns is still present in some elements of the loop; the origin for this delay is under investigation.

11.4 FFO Phase-Locking Directly by HM

The radical improvement of the described above CPLL system may be achieved by implementation of a single SIS junction as the HM and the phase detector simultaneously. This cryogenic harmonic phase detector (CHPD) substitutes the HM, the HEMT-amplifier, and the CPD in the CPLL (Fig. 11.3). The CHPD and all loop elements can be placed on the same chip with the FFO, which leads to further loop group delay reduction. Such a PLL system will be ultra-wideband. A block diagram of the new PLL system is shown in Fig. 11.6. The signals from the FFO and the LO#1 are applied to the CHPD. The frequency of harmonic of the LO#1 signal is equal to the FFO frequency (of the order of 600 GHz). The CHPD generates an output signal proportional to the phase difference between the FFO and the appropriate harmonic of the LO#1. This error signal is applied directly to the FFO control line through a low-pass filter. For demonstration of the CHPD operation, the additional SIS Mixer is used. This mixer operates as a HM (see Fig. 11.6). It is utilized for observation of the FFO radiation line spectrum and monitoring of the phase-locking effect. The LO#2 frequency is chosen to obtain the intermediate frequency (IF) of this mixer of about 6 GHz. Such an IF is determined by the operating range 4–8 GHz of the HEMT-amplifiers in IF chain of the SIS mixer.

11.4.1 On the Theory of HM

It is crucial to achieve a high-power output signal of the HM based on SIS to reach the effective FFO synchronization. The experimental data shows that power of the IF signal depends in a complicated way on the HM bias voltage, frequencies and powers of the LO and FFO signals. To study the HM properties, it has been theoretically analyzed and the 3D dependences of its output signal power versus the bias voltage of SIS junction and the LO power have been calculated. The

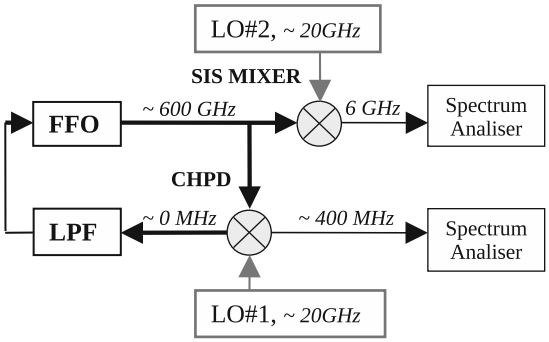

Fig. 11.6 Block diagram of the system for the FFO synchronization by the CHPD

detailed theoretical description of the SIS junction under action of microwave frequency signals is given in [12, 18, 19]. In [12], a simplifying assumption about the small amplitude of the input signal and shunting of the highest harmonics of the LO by junction capacitance was used. Papers [18, 19] involved the method of the SIS junction description in general case, that is for any powers of input signals. Nowadays the theory [18, 19] is the most complete; it takes into account existence of the harmonics generated by SIS junction and influence of the external electromagnetic environment. The calculations of some HM characteristics on the SIS based on this theory are given in [19].

We present the simplified model, which gives us the opportunity to reduce the time of HM characteristics calculation, but good qualitative and quantitative agreement with the experimental data still can be obtained. Let us consider the model of the weakly interacting quasi-particles under the influence of the periodic electric field without taking into account spin effects as in [20].

Wave function of a quasi-particle with energy E without applying high-frequency electric field is $\Psi = f(x, y, z)\exp(-\mathrm{i}Et/\hbar)$, where $f(x, y, z)$ – certain function of coordinates, i – imaginary unit, t – time, $\hbar$ – Planck's constant. This wave function is the eigen function of a nonexcited system Hamiltonian H_0. The voltage across the junction is $V_{\omega 1}\cos(\omega_1 t) + V_{\omega 2}\cos(\omega_2 t)$ then two periodic signals of frequencies ω_1, ω_2 and of amplitudes $V_{\omega 1}$, $V_{\omega 2}$ are applied to junction electrodes. The Hamiltonian of quasi-particles system is then:

$$H = H_0 + \mathrm{eV}_{\omega 1}\cos(\omega_1 t) + \mathrm{eV}_{\omega 2}\cos(\omega_1 t),$$

where H_0 – nonexcited system Hamiltonian, H – Hamiltonian of system influenced by two harmonic signals, e – charge of electron. The new wave function is:

$$\Psi = f(x, y, z)\exp(-\mathrm{i}Et/\hbar)\left(\sum_n B_n \exp(-\mathrm{i}n\omega_1 t)\right)\left(\sum_m C_m \exp(-\mathrm{i}m\omega_2 t)\right),$$

where B_n and C_m – unknown functions.

Applying this wave function to Schrödinger's equation

$$\mathrm{i}\hbar\frac{\partial\psi}{\partial t} = \widehat{H}\,\psi,$$

we obtain equations for B_n and C_m.

Solution of this Schrödinger's equation is:

$$\Psi = f(x)\exp(-\mathrm{i}Et/\hbar)\left(\sum_n\sum_m J_n\left(\frac{\mathrm{eV}_{\omega 1}}{\hbar\omega_1}\right)J_m\left(\frac{\mathrm{eV}_{\omega 2}}{\hbar\omega_2}\right)\exp\left[-\mathrm{i}(n\omega_1+m\omega_2)t\right]\right),$$

where $J_n(\alpha)$ Bessel function nth order

One can see that quasiparticles energy levels are split into levels described by wave functions Ψ_{nm} with energies $E + n\hbar\omega_1 + m\hbar\omega_2$; $n, m = 0, \pm1, \pm2\ldots$. Probability of occupation of such levels is proportional to $J_n\left(\frac{\mathrm{eV}_{\omega 1}}{\hbar\omega_1}\right)J_m\left(\frac{\mathrm{eV}_{\omega 2}}{\hbar\omega_2}\right)$.

Quasi-particle tunnel current is provided by quasiparticles transport between SIS junction electrodes. This current is described as complex function of current response $j(V)$, here V is a DC voltage applied to junction. The function $j(V)$ is calculated in [21]: $j(V) = \mathrm{i}I_{\mathrm{dc}}(V) + I_{\mathrm{KK}}(V)$. Here, $I_{\mathrm{dc}}(V)$ is unpumped I–V curve of the SIS, and the $I_{\mathrm{KK}}(V)$ relates to the $I_{\mathrm{dc}}(V)$ as Kramers–Kronig transform.

It should be noted that the experimentally measured $j(V)$ function was used in the calculations. The I–V curve of the HM contains all the information about the gap voltage, its smearing, the gap current (current step at the gap voltage), and leakage current below the gap.

The quasiparticle increases its energy by $\hbar\omega$ when the radiation quantum is absorbed. One can describe this process by application of the voltage $\hbar\omega/e$ to the junction. Therefore, the tunnel current is defined by function $j(V + \hbar\omega/e)$. As far as the quasiparticle is able to absorb several photons of the energy $\hbar\omega_1$ and $\hbar\omega_2$, in order to find the total tunnel current we should sum the current response functions $j_{\mathrm{nm}} = j\left(V + \frac{n\hbar\omega_1}{e} + \frac{m\hbar\omega_2}{e}\right)$ subject to the probability of the quasiparticle tunneling. The quasiparticle transmission probability of state Ψ_{nm} to state Ψ_{lk} is defined by the matrix element $\langle\Psi_{\mathrm{lk}}|\Psi_{\mathrm{nm}}\rangle$, where

$$|\Psi_{\mathrm{nm}}\rangle = f(x)\exp(-\mathrm{i}Et/\hbar)\left(J_n\left(\frac{\mathrm{eV}_{\omega 1}}{\hbar\omega_1}\right)J_m\left(\frac{\mathrm{eV}_{\omega 2}}{\hbar\omega_2}\right)\exp\left[-\mathrm{i}(n\omega_1+m\omega_2)t\right]\right),$$
$$\langle\Psi_{\mathrm{lk}}| = g(x)\exp(-\mathrm{i}Et/\hbar)\left(J_l\left(\frac{\mathrm{eV}_{\omega 1}}{\hbar\omega_1}\right)J_k\left(\frac{\mathrm{eV}_{\omega 2}}{\hbar\omega_2}\right)\exp\left[\mathrm{i}(l\omega_1+k\omega_2)t\right]\right).$$

The changing of the summation variable leads to:

$$I(V,t) = \mathrm{Im}\sum_{n,m,l,k} J_n(\alpha_1)J_{n+l}(\alpha_1)J_m(\alpha_2)J_{m+k}(\alpha_2)^* \\ *\exp\left[-\mathrm{i}(l\omega_1+k\omega_2)t\right]j\left(V+\frac{n\hbar\omega_1}{e}+\frac{m\hbar\omega_2}{e}\right),$$

where $\alpha_i = \frac{\mathrm{eV}_{\omega i}}{\hbar\omega_i}$.

It should be noted that we can overwrite the current function in the form:

$$I(V,t) = a_0 + \sum_{l=1}^{\infty}\sum_{k=1}^{\infty}(2a_{lk}\cos((l\omega_1 + k\omega_2)t) + 2b_{lk}\sin((l\omega_1 + k\omega_2)t)).$$

This formula shows that the signals of the frequencies described as $l\omega_1 + k\omega_2$ (l and k are integers) are generated on the SIS junction. For the practical application of the HM, the first signal frequency is close to the frequency of second signal harmonic k, i.e. $l = 1$ and $\omega_1 - k\omega_2 << \omega_2$. Let us put that frequency of RF signal is $\omega_1 \equiv 2\pi f_{\mathrm{RF}}$, and for LO signal is $\omega_2 \equiv 2\pi f_{\mathrm{LO}}$. Then current amplitude of IF $f_{\mathrm{IF}} = f_{\mathrm{RF}} - nf_{\mathrm{LO}}$ is given by

$I_{\mathrm{IF}} = \sqrt{{a_{1k}}^2 + {b_{1k}}^2}$, here

$$a_{1k}(V) = \sum_{n,m} J_n(\alpha_1)J_m(\alpha_2)\left[J_{n+1}(\alpha_1)J_{m-k}(\alpha_2) + J_{n-1}(\alpha_1)J_{m+k}(\alpha_2)\right] \times I_{\mathrm{dc}}\left(V + \frac{n\hbar\omega_1}{e} + \frac{m\hbar\omega_2}{e}\right),$$

$$b_{1k}(V) = \sum_{n,m} J_n(\alpha_1)J_m(\alpha_2)\left[J_{n+1}(\alpha_1)J_{m-k}(\alpha_2) - J_{n-1}(\alpha_1)J_{m+k}(\alpha_2)\right] \times I_{\mathrm{kk}}\left(V + \frac{n\hbar\omega_1}{e} + \frac{m\hbar\omega_2}{e}\right).$$

The dependences of the IF signal power versus the input signals parameters and the junction bias voltage have been calculated by the presented formula. The result of such calculations is shown in Fig. 11.7 (top part).

The experimental study of such dependences is also performed. In Fig. 11.7 (bottom part), there is a dependence of the IF power versus LO power and bias voltage for the RF signal frequency 636 GHz and the LO frequency 18 GHz. Good qualitative and quantitative correspondence between theory and experiment is achieved (Fig. 11.7). The Nb–AlOx–Nb SIS junction with area of 1 μ^2 and gap current 90 μA was used in the experiment. The maximum output signal power of about −90 dBm has been obtained for described frequencies. However, the calculations show that 5 dB larger value would be achieved at more careful adjustment.

11.4.2 Experimental Demonstration

A test circuit presented by the diagram in Fig. 11.6 has been experimentally realized. The feedback loop between the HM and the FFO was implemented in two ways: by lumped elements on a contact plate and by the microstrip lines directly on the chip.

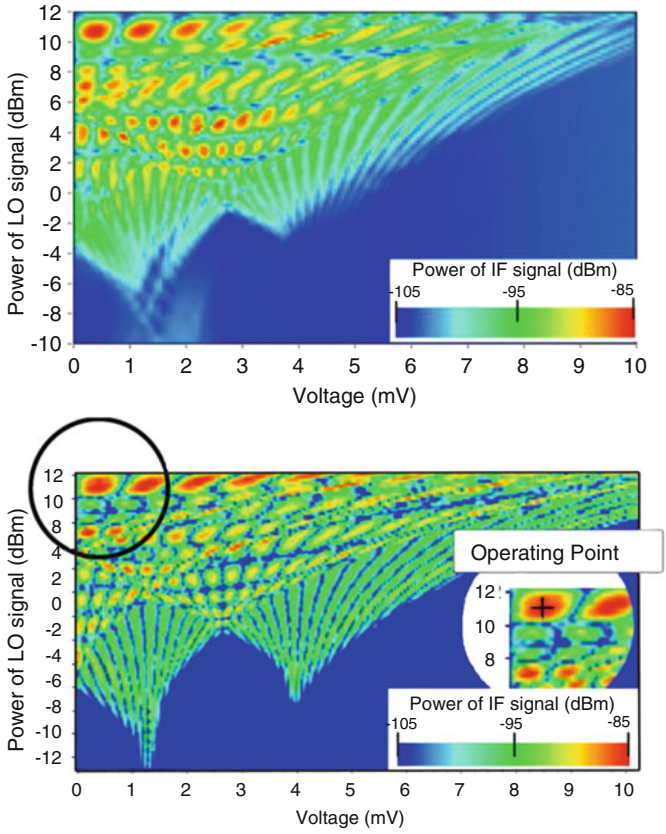

Fig. 11.7 Experimental (*up*) and theoretical (*bottom*) dependence of IF signal's power versus LO signal's power and bias voltage across the HM. The operating point with the maximum power of IF signal (−85 dBm) is shown on the theoretical dependence. The FFO frequency is 636 GHz, LO frequency – 18 GHz (the 35th harmonic of LO is used) as result frequency of IF signal is equal 6 GHz. The critical current of the SIS junction was suppressed by the magnetic field

In the experiment, the FFO signal is split into two channels to pump both mixers. Each part of the signal is downconverted, so that output signals frequencies are 400 MHz for the CHPD and of about 6 GHz for the SIS (Fig. 11.6). At the first stage of the experiment, the CHPD output signal is observed at 400 MHz by the spectrum analyzer and is maximized by determining of the optimal operating point (see Fig. 11.7). After the optimum is found, the LO#1 frequency is tuned so that the IF of the CHPD becomes "0" instead of 400 MHz and the FFO becomes phase-locked. At the same time, the IF of the HM #2 is also changed but the FFO radiation line is still presented on spectrum analyzer screen and synchronization effect is observed.

The result of the FFO synchronization by the CHPD is shown in the Fig. 11.8. This spectrum demonstrates the validity and the potential of the concept. The group

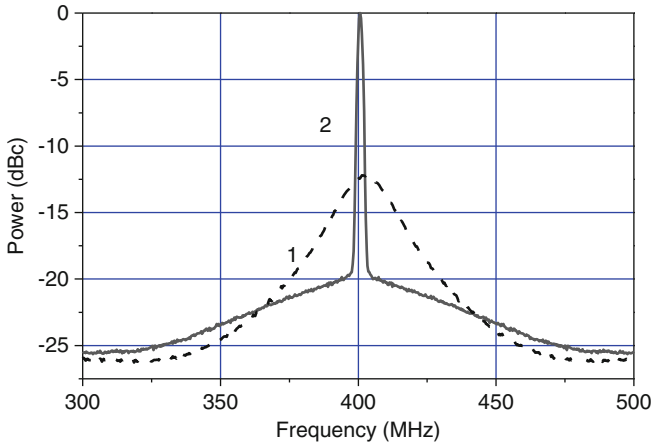

Fig. 11.8 Downconverted spectrum of the FFO: curve "1" – free running line, LW about 20 MHz; curve "2" – FFO is phase-locked by the CHPD

delay of the loop is less than 2 ns, and the bandwidth of such a PLL system is expected to be about 100 MHz. For the data presented in Fig. 11.8 (curve "1"), free running FFO linewidth is about 20 MHz and the PLL system based on CHPD can phase-lock as much as 70% of the emitted FFO power (curve "2"). According to the scale effect, described for Fig. 11.5, the BW of such a PLL system should be also about 100 MHz. However, the HM output signal is limited and the open loop gain is not large enough to for the optimal synchronization. As a result, the phase noise shoulders like in the Fig. 11.4 demonstrating BW are not observed and the maximum SR is not achieved.

11.5 Conclusions

The concept of the ultra-wideband CPLL system based on the CPD has been developed and experimentally proven. The CPD based on the SIS junction has been studied in detail. Synchronization bandwidth as large as 40 MHz has been realized for cryogenic PL; that considerably exceeds the value of about 12 MHz obtained for regular room-temperature PLL. The innovative CPLL system can phase-lock more than 50% of the FFO spectral line if the free-running FFO is about 12 MHz. Practical implementation of the CPLL looks especially promising for phase-locking of new superconducting LOs utilizing NbN/NbTiN films, as well as for SIR applications in the interferometry where the extremely low LO phase noise is required.

The novel application of the SIS junction – the CHPD has been proposed. The theoretical and experimental studies of the HM are performed. Comparison of the theoretical and experimental data demonstrates a good qualitative and quantitative

agreement. The concept of the CHPD is experimentally realized and the FFO phase-locking has been obtained. The part of the phase-locked FFO power is not ultimate because output signal of HM was not large enough. This problem would be overcome by utilizing the HM with larger area.

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