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# A cryogenic phase locking loop system for a superconducting integrated receiver

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## Abstract

The authors present a new cryogenic device, an ultrawideband cryogenic phase locking loop system (CPLL). The CPLL was developed for phase locking of a flux-flow oscillator (FFO) in a superconducting integrated receiver (SIR) but can be used for any cryogenic terahertz oscillator. The key element of the CPLL is the cryogenic phase detector (CPD), a recently proposed new superconducting element. The CPD is an innovative implementation of a superconductor–insulator–superconductor tunnel junction. All components of the CPLL reside inside a cryostat at 4.2 K, with the loop length of cables 50 cm and the total loop delay 4.5 ns. So small a delay results in a CPLL synchronization bandwidth as wide as 40 MHz and allows phase locking of more than 60% of the power emitted by the FFO, even for FFO linewidths of about 11 MHz. This percentage of phase locked power is three times that achieved with conventional room temperature PLLs. Such an improvement enables reducing the FFO phase noise and extending the SIR operation range.

(Some figures in this article are in colour only in the electronic version)

## 1. Introduction

A cryogenic phase locking loop system (CPLL) is primarily intended for phase stabilization of a local oscillator (LO) of a superconducting integrated receiver (SIR) [1, 2]. The SIR circuit embodied on a chip (of size 4 mm × 4 mm × 0.5 mm) comprises a low noise SIS (superconductor–insulator–superconductor) mixer with quasioptical planar antenna, a superconducting flux-flow oscillator (FFO) acting as a tunable LO in the frequency range 400–700 GHz and a second SIS harmonic mixer (HM) to phase lock the FFO.

The FFO emission spectrum was found to be the Lorentz line [3, 4] at frequencies up to 750 GHz. Such a line shape indicates that the free-running ('natural') FFO linewidth is determined by the wideband noise, i.e., thermal fluctuations and the shot noise. This is contrary to the case for many traditional microwave oscillators (for example, backward-wave

and Gunn oscillators), where the 'natural' linewidth is rather narrow and is broadened primarily by external fluctuations. In fact, the FFO linewidth may be up to 10 MHz. Therefore, for higher spectral resolution, the FFO frequency should be stabilized with a wideband phase locking loop system (PLL). The wider the PLL synchronization bandwidth (BW), the greater the amount of power of the FFO that can be phase locked (PL), resulting in lower phase noise. The ratio of the phase locked power to the total power emitted by the oscillator is called the 'spectral ratio' (SR). Actually, the SR is determined from a measured LO spectrum as the ratio of the phase locked power of the carrier to the total emitted power comprising the carrier and the intrinsic phase noise power generated by the LO [4]. Usually the noise power is embedded in the bandwidth, 100 MHz. An example of a PL FFO spectrum is presented in figure 3. So, the SR would be 100% for an ideal LO with a delta-shaped spectrum and

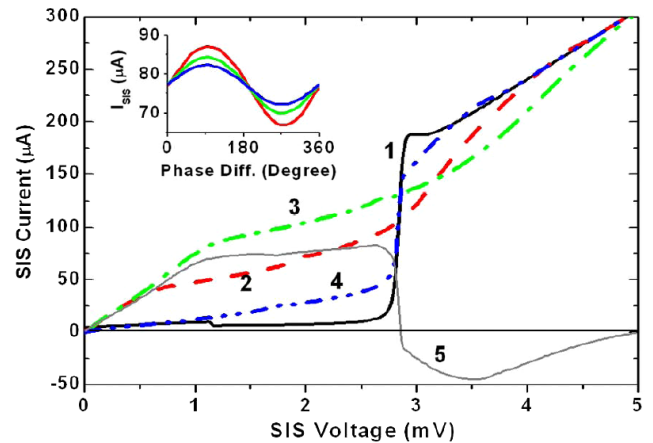
zero phase noise level. Note that phase noise measured at large offsets from the carrier (about 50 MHz) is primarily due to an IF amplifier, and we do not subtract this level in SR calculations (so the actual SR is even a little higher). The error introduced due to measurement of the carrier power by a spectrum analyzer with the resolution bandwidth of 1 MHz is about 1–3%.

For FFO phase locking a specially designed semiconductor room temperature PLL (RT PLL) with a BW of about 12 MHz is used. The RT PLL provides an SR value of about 50% for the 5 MHz wide FFO emission line.

There are several reasons for extending the BW of the PLL system much beyond the present 12 MHz. The first is that at voltages exceeding a third of the FFO gap voltage, where the Josephson self-coupling effect drastically modifies FFO IVCs, increasing the differential resistance and internal damping [5, 6], the FFO linewidth exceeds 10 MHz. In the case of such a wide line, an essential part of the emitted FFO power cannot be phase locked with the RT PLL (the SR is as low as 20–25%). The second reason is that FFOs based on NbN or NbTiN films are the most attractive for future SIR applications at frequencies of about 1 THz. The linewidth of such FFOs can considerably exceed 10 MHz due to higher surface losses. In this situation the PLL bandwidth has to be as large as 50 MHz (to reach at least 50% of the SR value required for most applications). The third reason is that using the SIR for interferometry applications requires an LO with extremely high phase stability. For example, for the ALMA project (an interferometer in Chile with up to 15 km baseline) the LO rms phase noise should be considerably less than 75 fs (the value of rms atmospheric fluctuation at interferometer site) [7]. The required value of the SR for this rms phase noise level at the frequency of about 600 GHz is over 95%. To provide such a high SR value even for the FFO with relatively narrow linewidth of 2 MHz, the PLL should have a BW of about 50 MHz.

The BW is determined by the group delay  $\tau$  in the loop [8, 9]. It should be emphasized that the noise of RT PLL elements is low enough as compared to the noise of the IF amplifier and it does not affect the phase locking efficiency. For the RT PLL, the BW is limited to 12 MHz due to the total delay of about 15 ns (including a 5 ns contribution from the PLL filters and semiconductor electronics and 10 ns from the 2 m long cables connecting the RT PLL electronics with cryogenic FFO). The minimal cabling length is restricted by the size of a cryostat and cannot be essentially reduced without increasing the heat flux into the cryogenic space. Note that the traditional PLL is a semiconductor-based device designed for 300 K, and it cannot be placed directly into the cryostat.

To improve the spectral characteristics of the FFO and to overcome the limitation of the RT PLL, we propose a cryogenic phase locking loop system (CPLL) based on a cryogenic phase detector (CPD) [8, 9]. All elements of the CPLL can be located very close to the FFO inside the cryostat to avoid any temperature gradients between the FFO and phase detector and to minimize the loop length. The negligible CPD delay and small time delays in the short loop enable an ultrawide BW.



**Figure 1.** IVCs of the SIS junction measured at various settings of the microwave signals (frequency 5 GHz): curves '1'—autonomous; '2'—pumped by one microwave signal; '3'—pumped by two in-phase microwave signals; '4'—pumped by two anti-phase microwave signals (PSynth1 = 0.3  $\mu$ W, PSynth2 = 0.1  $\mu$ W); '5'—phase response of the CPD. The inset shows a sinusoidal dependence of the SIS current versus phase difference between the signals.

## 2. A cryogenic phase detector

A key element of the CPLL is the CPD based on a micron-sized SIS tunnel junction. A principle of CPD operation can be demonstrated by the junction IVCs. The IVC of a typical autonomous SIS and the IVC of a SIS pumped by a microwave signal are shown in figure 1 (curves 1 and 2). Two microwave signals applied in phase give higher power and a higher pumping level (curve 3), while anti-phase results in lower pumping level (curve 4). The difference between curve 3 and curve 4 represents the phase response. It is important that the shape of the pumping current versus the phase difference of two applied signals is sinusoidal in a real experimental environment [8]; see the inset to figure 1. Numerous experiments evidence that the optimal bias voltage for CPD operation is in the range of 2–2.5 mV.

The CPD is a unique phase detector due to the non-linearity of the SIS junction [10]. Although the frequency of the synthesizer for curves 2–4 is a few GHz (which is rather low compared to the smearing of the superconducting gap), the shape of the pumped CPD *IV*-curve looks very much like a result of irradiation by a high frequency signal. Apparently, a certain number of higher order harmonics of the applied signal are excited in the SIS junction due to its non-linearity; these harmonics effectively pump the tunnel junction. We have compared both experimental IVCs and the dependence of the CPD pump current as a function of power of the applied signal with the simulated ones. Calculations were performed on the basis of the Tien–Gordon formula for photon-assisted tunneling (see e.g. [10]). The best fit to the experimental results was found for frequencies of the applied signal in the range of 80–100 GHz; at that, the shape of experimental curves qualitatively resembles the theoretical ones for synthesizer frequency in the range of 0.4–20 GHz. Due to small SIS capacitance at the CPD input frequencies in the range specified

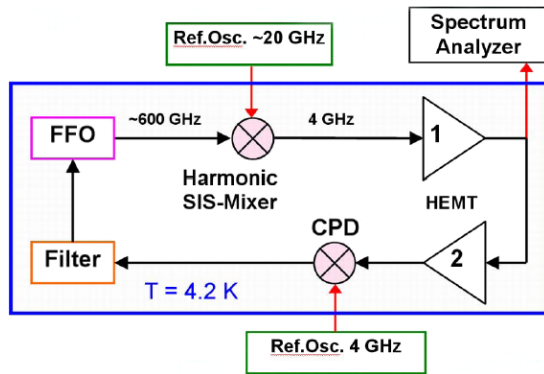


Figure 2. Flow chart of the CPLL for FFO phase locking.

above, the magnitude of the CPD response remains at the same level at least in the frequency range up to 750 MHz [9], which essentially exceeds the 100 MHz required for the CPLL operation.

### 3. A cryogenic phase locking loop system: description and experimental results

We have developed and tested several experimental embodiments of the CPLL systems with various operation frequencies and various loop lengths. A flowchart of the latest design is shown in figure 2. The FFO emission at the frequency of the order of 600 GHz is downconverted by the harmonic mixer (HM) to the frequency 4 GHz and amplified by two HEMT amplifiers, HEMT 1 and HEMT 2. This signal is compared with the external reference signal by the CPD and the resulting output error signal (proportional to the phase difference) is applied to the FFO to control its frequency. A certain fraction of the microwave power after HEMT 1 is tapped by the directional coupler to the spectrum analyzer. A filter between the CPD and the FFO comprises a rejecter filter to suppress signals close to the reference frequency and an integrating loop filter for locking and holding of the FFO frequency.

In the latest design the loop length has been reduced to 50 cm, which corresponds to a delay of 2.5 ns. The operating frequency for this system was chosen as 4 GHz. For such a frequency, a band-stop filter (between CPD and FFO) with delay less than 0.5 ns has been developed. The reduction of the loop delay due to the described modifications results in increasing of the BW up to 40 MHz (see figure 3, curve 2).

In figure 3, downconverted spectra of the FFO phase locked by different PLL systems are presented (the spectrum of the free-running FFO is also shown for comparison). It should be noted that all phase locked spectra have a typical shape consisting of a central peak containing locked power and phase noise shoulders on the sides of the peak. For example, the tops of the shoulders for the CPLL with BW 40 MHz are located at offsets 35–40 MHz from the carrier (curve 2 in figure 3). At these frequencies the phase of the return signal is shifted by  $\pi$  due to the delay in the loop, and instead of noise suppression, increasing of the phase noise occurs in the PLL system; the positions of these shoulders allow estimation of the PLL BW.

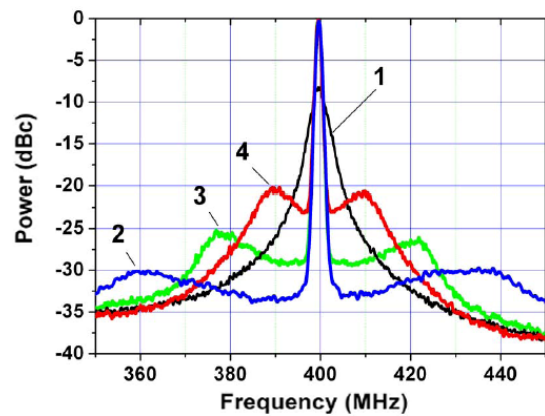


Figure 3. Downconverted spectra of the FFO operating at 600 GHz: curves '1'—free running, linewidth 2 MHz; '2'—phase locked with CPLL, BW 40 MHz (SR = 94%); '3'—phase locked with CPLL, BW 25 MHz (SR = 91%); '4'—phase locked with RT PLL, BW 12 MHz (SR = 82%).

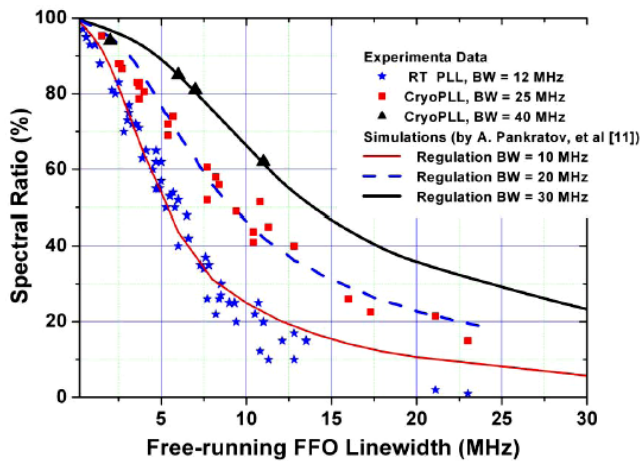
These shoulders rise and become sharp with increasing of the PLL loop gain. The optimal PLL gain for any given PLL system is achieved for the shoulders about 3 dB higher than the phase noise near the carrier. In this case the maximal SR and signal to noise ratio are reached.

From figure 3 one can see that increasing of the PLL BW leads to expansion of the frequency range, where the phase noise of the PL FFO is lower than the level for the free-running FFO. The reason is that the wider BW of the CPLL enables using higher loop gain, bringing about an essential reduction of the phase noise over the entire regulation bandwidth (the frequency of unit gain is shifted to the right) without considerable increase of the phase noise in the shoulders.

For the FFO linewidth of 2 MHz, the CPLL is capable of phase locking with 94% power, as compared to 82% for the RT PLL (figure 3). For the FFO linewidth of 7 MHz, the new CPLL yields SR = 81% instead of 41% for the RT PLL. Even higher gain was obtained at a broader linewidth of 11 MHz for a free-running FFO: SR = 63% in the case of CPLL against 23% for RT PLL.

A summary of the results obtained is presented in figure 4. Experimental data for the RT PLL with the BW of 12 MHz are shown by asterisks, for the CPLL with BW 25 MHz by squares, and triangles show results for the CPLL described with BW of 40 MHz. Lines show results of numerical simulations [11], to fit the experiment. The 'regulation BW' of 10 MHz in simulations roughly corresponds to 'BW' = 12 MHz in experiment. Data for the CPLL described are shown as a solid line (effective regulation BW of 30 MHz in simulations); these data show the advantage of BW broadening and prospects for future improvement. It can be expected that a double-width FFO line could be phase locked by the PLL with double-width BW resulting in the same SR. Experimental data analysis demonstrates that the relative fraction of the phase noise ( $1 - \text{SR}$ ) falls linearly with BW increasing at  $\text{SR} > 50\%$ .

It should be noted that the overall group delay for the CPLL described is estimated as 3 ns, but both BW and SR measurements indicate the delay of about 4.5 ns. This means that the additional delay of about 1.5 ns is still present in



**Figure 4.** SR versus FFO linewidth for PLL systems with various synchronization bandwidths.

some elements of the loop; the origin for this delay is under investigation.

#### 4. Conclusion

The concept of an ultrawideband cryogenic phase locking loop system based on a cryogenic phase detector has been developed and experimentally proven. Synchronization bandwidths as large as 40 MHz have been implemented in operation with a cryogenic FFO, which considerably exceeds the value of about 12 MHz obtained for the regular room temperature PLL. The innovative CPLL system can phase lock more than 50% of the FFO spectral line if the free-running FFO is about 12 MHz. Practical implementation of the CPLL looks especially promising for phase locking of new superconducting local oscillators utilizing NbN/NbTiN films, as well as for SIR applications in the interferometry where the extremely low LO phase noise is required.

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