Cryogenic Phase Locking Loop System for Flux Flow Oscillator

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Abstract

A bandwidth of the typical Phase Locking Loop (**PLL**) system for the Superconducting Integrated Receiver (**SIR**) is limited by unavoidable delays in the long cables between SIR inside cryostat semiconductor PLL system outside it. To overcome this limitation we propose Cryogenic Phase Locking Loop (**CPLL**).The CPLL has been developed for phase locking of a Flux-Flow Oscillator (**FFO**) in the SIR. The main element of the CPLL is a cryogenic phase detector (**CPD**) based on a superconductor – insulator – superconductor (SIS) tunnel junction.

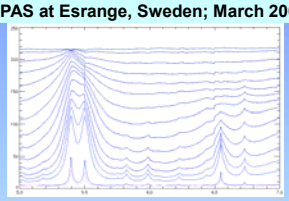
All the loop elements are placed at 4.2 K inside a cryostat with the FFO; so the novel CPLL system has a loop length only 50 cm. The CPLL operating frequency has been increased from 400 MHz up to 4 GHz to decrease a loop filter delay to 0.5 ns. As a result the total loop group delay is about 4.5 ns. Such a small delay results in a CPLL synchronization bandwidth as wide as 40 MHz and allows to phase-lock more than 60% of the emitted by FFO power even for FFO linewidth about 11 MHz. This fraction of phase-locked power is three times large than can be achieved with conventional room-temperature PLL. We have realized an integrating loop filter for the CPLL. Such a filter sufficiently increase stability and decrease a phase noise of the FFO phase-locked by the CPLL.

Frequencies and substances selected for the first TELIS flight

##	FFO Frequency, GHz	Substances (High priority)
1	495.04	$H_2{}^{18}O$
2	496.88	HDO
3	505.6	BrO (ΔT = 0.3 K !!)
4	507.28	ClO
5	515.25	O_2 /pointing /pressure
6	519.25	BrO (ΔT = 0.3 K !!)
7	607.78	O_3 isotopes
8	619.1	HCl (HOCl, ClO)

TELIS: successful flight of 12 hours on 30 kilometers altitude! The SIR developed by SRON and IREE for TELIS has been able to measure the ozone depleting component brome oxide in the stratosphere from a gondola of high–altitude balloon. The SIR channel provided valuable scientific data during the whole flight; these data are under elaboration right now.

TELIS-MIPAS at Esrange, Sweden; March 2009

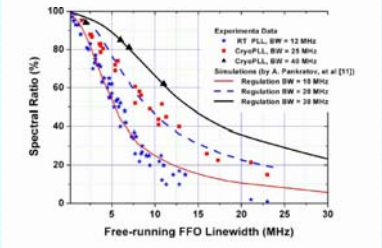


Example of measured atmospheric spectra.

Ultrawideband PLL is required (>50 MHz):

For the future SIR applications (f>1THz) an FFO with the NbN electrodes will be used; the FFO linewidth could considerably exceed 10 MHz.

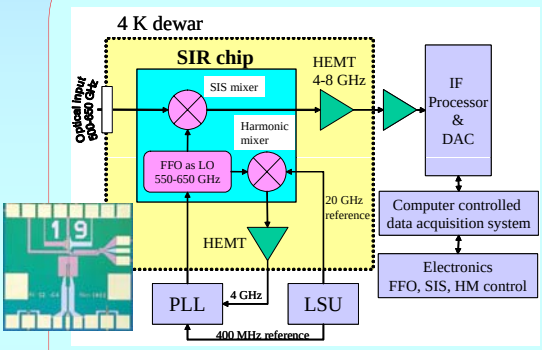
The specification for a ALMA interferometer require a phase stability better then 75 fs. To realize such a stability for the SIR a part of phase locked FFO power – **Spectral Ratio (SR),** as high as 90% is needed.



Dependence of the SR vs FFO linewidth for different PLL bandwidths.

The PLL bandwidth is determined by a total group delay in the loop. A bandwidth of the typical PLL system for the SIR is limited by unavoidable delays in the long cables between the SIR inside a cryostat and semiconductor PLL system outside it. To overcome this limitation we propose the CPLL.

Superconducting Integrated Receiver

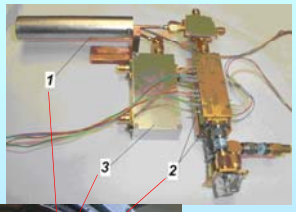


Schematics of the FFO stabilization circuit. FFO frequency is mixed in HM with the 19-21 GHz reference. The mixing product is amplified, downconverted and compared with the 400 MHz reference in the PLL. The phase difference signal generated by PLL is used to feedback the FFO control line.

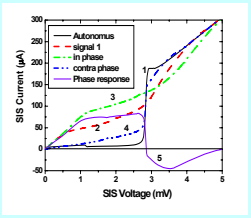
CPLL Loop Elements:

1 - FFO with HM in shield
2 - HEMT amplifiers
3 - CPD and Loop filter in the box

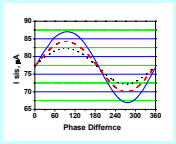
Loop length is 0.5m.



SIS - Cryogenic Phase Detector for the CPLL

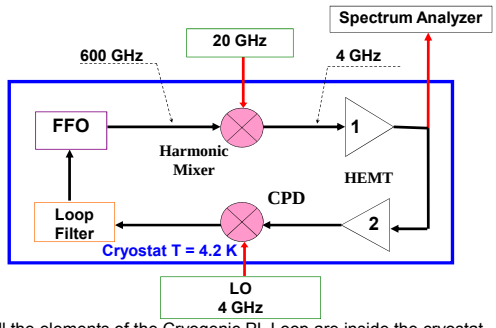


I-VCs of a SIS junction. Microwave signals (5 GHz) are applied.



CPD based on SIS demonstrates sinusoidal response in dependence on phase difference between two incoming microwave signals.

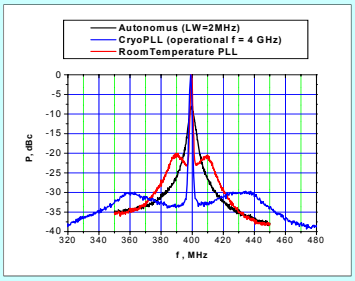
Concept of the Cryogenic PLL



All the elements of the Cryogenic PL Loop are inside the cryostat with a FFO. It allows to minimize the loop length and the time delay.

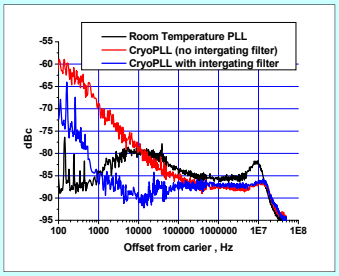
Photo of the CPLL in cryostat. FFO and CPD are placed in two separated shields.

Results for FFO phase-locking with CPLL



Downconverted spectra of FFO. Demonstration of the CPLL advantage: bandwidth = 40 MHz it gives SR = 95% for 2 MHz linewidth compare to SR=82% for the Room Temperature PLL system.

	RoomPLL	CryoPLL
Loop length(м)	2	0.5
Delay in elements (ns)	5	2
Total Delay (ns)	15	4.5
Bandwidth (MHz)	12	40!



Phase noise of the FFO phase-locked with: "1" –RT PLL; "2" – CPLL without integrating loop filter; "3" - CPLL with integrating loop filter. The CPLL demonstrate a Phase Noise lower then for the Room Temperature PLL at frequencies more then 1kHz .

Summary

- A new and successful application of a SIS junction - cryogenic phase detector (CPD).
- The CPD intrinsically could operate with an effective bandwidth more than 100 MHz. The maximal output signal is about 0.1 mV.
- Concept of the CryoPLL system has been proven. Bandwidth as wide as 40 MHz has been obtained.
- The improvement of the phase locked FFO spectral ratio from 20% to more than 60% has been achieved at application of the CryoPLL for FFO linewidth 11 MHz.
- CryoPLL has an integrating filter for active phase-locking, stabilization and low phase level noise.

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