CRYOGENIC PHASE LOCKING LOOP SYSTEM FOR SUPERCONDUCTING INTEGRATED RECEIVER

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***Abstract*—Recently a Cryogenic Phase Locking Loop system (CPLL) has been proposed and successfully tested. The CPLL is intended for phase locking of a Flux-Flow Oscillator (FFO) in a Superconducting Integrated Receiver (SIR). The CPLL based on a cryogenic phase detector (CPD) demonstrate much wider bandwidth than that of its prototype conventional room-temperature PLL system based on semiconductor elements. In this article we present new experimental results achieved with the last realization of the CPLL. This CPLL has operation frequency 4 GHz and the loop length is about 50 cm. The total time delay in the loop is about 4.5 ns that results in a CPLL synchronization bandwidth as much as 40 MHz. The novel CPLL system can phase-lock more than 60% of the emitted by FFO power even if the free-running FFO linewidth is about 11 MHz. This fraction of phase-locked power is three times more than can be achieved with the conventional room-temperature PLL. Such an improvement allows reducing the FFO phase noise and extending the SIR operation range.**

***Index Terms*—Phase detection, phase locked loops, phase synchronization, superconducting integrated circuits, superconductor-insulator-superconductor devices**

I. INTRODUCTION

A Cryogenic Phase Locking Loop system (CPLL) is primarily designed for phase stabilization of a Local Oscillator (LO) of a Superconducting Integrated Receiver (SIR) [1], [2]. The SIR circuit comprises on a one chip (size of 4 mm*4 mm*0.5 mm) a low noise SIS (superconductor – insulator - superconductor) mixer with quasioptical planar antenna, a superconducting Flux Flow Oscillator (FFO) acting as a tunable Local Oscillator (LO) in the frequency range 400 - 700 GHz and a second SIS harmonic mixer (HM) to phase-lock the FFO.

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The shape of the FFO radiation spectral line was found to be Lorentian [3], [4] at the frequencies up to 750 GHz. Such a shape indicates that the free-running ("natural") FFO linewidth is determined by the wideband noise, i.e. thermal fluctuations and the shot noise and may be up to 10 MHz. It differs from many traditional microwave oscillators (for example, backward-wave and Gunn oscillators) where the "natural" linewidth is rather small and is broadened mainly by external fluctuations. A specially designed wide-band phase locking loop (PLL) has been developed for stabilization of the FFO frequency [4]. The effective synchronization bandwidth (BW) of the existing room temperature PLL (RT PLL) is about 10 MHz. The so-called "spectral ratio" (SR) is the ratio between the phase-locked and the totally emitted by oscillator power. The wider PLL BW is the more power of the FFO can be phase-locked (resulting in higher SR). The RT PLL provides SR value around 50% for the 6 MHz wide FFO radiation line. The rest of the power gives impact directly into the LO phase noise. Intense phase noise is unacceptable for most SIR applications. Development of a special super-wideband PLL is a way to reduce the FFO phase noise (along with decreasing of the FFO free-running linewidth).

There are several reasons to extend the BW of the PLL systems to values much higher than the present 10 MHz for RT PLL. The FFO linewidth exceeds 10 MHz at the voltages above the one third of the FFO gap voltage, where the Josephson self-coupling effect drastically modifies FFO IVCs increasing differential resistance and internal damping [5], [6]. In case of such a wide line an essential part of the emitted FFO power can not be phase-locked with the RT PLL (the SR is only about 20 – 25 %).

FFOs based NbN or NbTiN films are the most attractive for future SIR applications at the frequencies around 1 THz. The linewidth of such FFOs can considerably exceed 10 MHz due to higher surface losses. In this situation the PLL has to have the bandwidth as large as 50 MHz (to reach the SR value at least 50% desirable for most applications).

Using an SIR for interferometry applications requires an LO with high phase stability. For example, for ALMA project (interferometer in Chile with the up to 15 km base line) the LO rms phase noise should be considerably less than 75 fs (the value of rms atmospheric fluctuation in location of the interferometer) [7]. The relationship between the rms phase noise and SR of the phase-locked LO for frequency 600 GHz is demonstrated in Fig. 1. From this dependence one can estimate that the SR > 95 % is required for ALMA

applications. To provide such a large SR value for the FFO with linewidth of 2 MHz the PLL should have BW about 50 MHz.

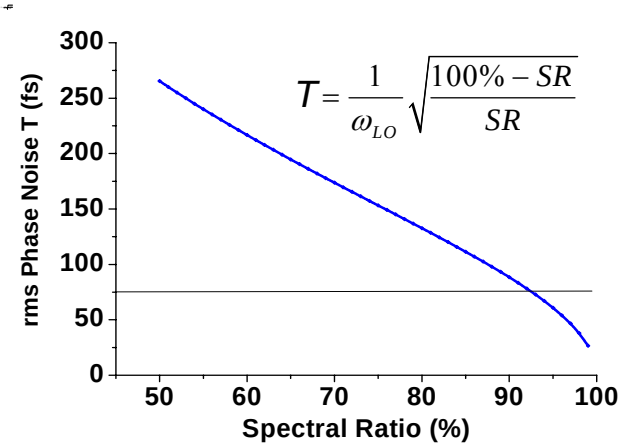

Fig. 1. Dependence of the rms phase noise value vs SR at ω_{LO} = 600 GHz.

II. Concept of the Cryogenic Phase-Looking Loop System

The PLL BW is determined by the group delay τ in the loop of the system. The BW of the existing RT PLL is limited to 12 MHz, because the τ is about 15 ns, including 5 ns contribution from the PLL filters and semiconductor electronics and 10 ns from delay in the 2 m long cables connecting the RT PLL electronics with the HM and the FFO. The minimal length of the cabling is restricted by the geometric size of a cryostat and can not be essentially reduced without increasing the heat flux into the cryogen space. From the other hand the traditional PLL can not be placed directly into the cryogenic volume inside the cryostat, as it is a semiconductor-based device designed for room temperature.

To improve spectral characteristics of the FFO and to overcome the limitation of RT PLL the Cryogenic Phase Locking Loop system (CPLL) based on a Cryogenic Phase Detector (CPD) has been proposed and successfully tested [8] – [10] (see diagram in Fig. 2). All elements of the CPLL can be placed very close to the FFO inside the cryostat to avoid any temperature gradients between FFO and phase detector and to minimize the loop length. Negligible delay in the CPD and small time delays in the short loop lead to ultra wide BW.

The CPD based on a well-developed tunnel SIS junction is a key element of the CPLL. The CPD is a unique phase detector because of SIS junction nonlinearity [11]. The experimental tests demonstrate that dependence of the phase response versus the phase difference between the two signals can be sinusoidal for the CPD under proper experimental circumstances [8]. The CPD input frequency can be ranged from 200 MHz to 20 GHz and the response amplitude remains flat at least up to 750 MHz, that considerable exceeds 100 MHz required for the CPLL operation [10].

A block diagram of the CPLL is shown in Fig. 2. The FFO radiation of the frequency around 600 GHz is down converted by the harmonic mixer (HM) to the frequency 4 GHz (400 MHz for the previous realization) and amplified by the two HEMT-amplifiers HEMT 1 and HEMT 2. This signal is compared by the CPD with the external reference signal and the resulting output error signal is proportional to the phase difference and fed to the FFO via the channel of the I_{CL} current. Some part of the microwave power after HEMT 1 is spitted by the directional coupler to the spectrum analyzer and can be also used as the input of the RT PLL and Frequency Detector, FD (the RT PLL and FD can operate together with the CPLL). It makes possible to stabilize the FFO frequency by the RT system mounted outside the cryostat. The filter between CPD and FFO blocks the signals around reference frequency. For better filter reflection a bigger value of reactive elements or higher number of them is necessary, but it leads to an increasing of the delay, so for these two parameters a trade off should be found.

The previous realization of the CPLL has been presented very recently [10]. This system has the length of the loop about 1 m (group delay 5 ns). The delay in filter is about 1.5 ns. There is also a delay 1 - 1.5 ns in other elements of the loop. So the total delay τ is 7 - 8 ns (compare to 15 ns for the RT PLL). This reduction of the τ results in increasing of the BW from 12 MHz to 25 MHz (see Fig. 4 curve 3). At the FFO linewidth of 2 MHz this CPLL is able to phase-lock 91% of the FFO power, compare to 82% for the RT PLL.

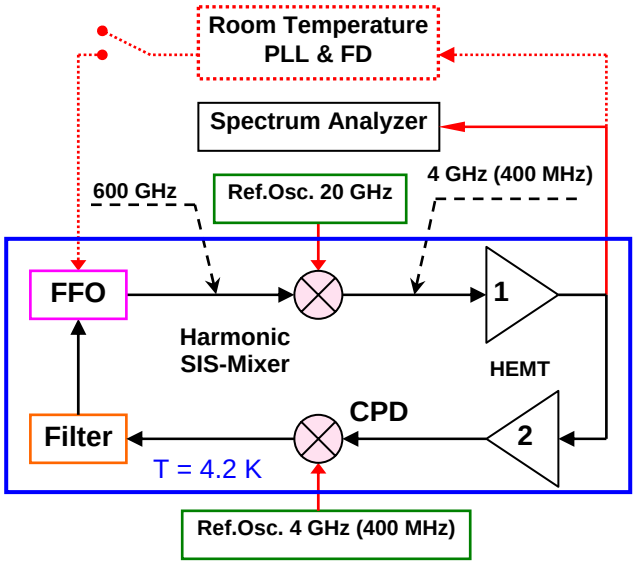

Fig. 2. Block diagram of the CPLL for FFO phase locking.

III. Experimental Results

Quite successful results obtained for the previous CPLL realization [10] encourage us for further attempts to reduce total delay in the loop. Firs of all we decrease further the loop length down to 50 cm that corresponds to delay 2.5 ns (see Fig. 3). As the next step of the CPLL development we considerably increase operational frequency of the system: from 400 MHz to 4 GHz. This modification gives us an opportunity to minimize delay introduced by band-stop filter due to smaller values of reactive elements needed to realize required filter reflection. Calculated delay in this new filter is about 0.5 ns.

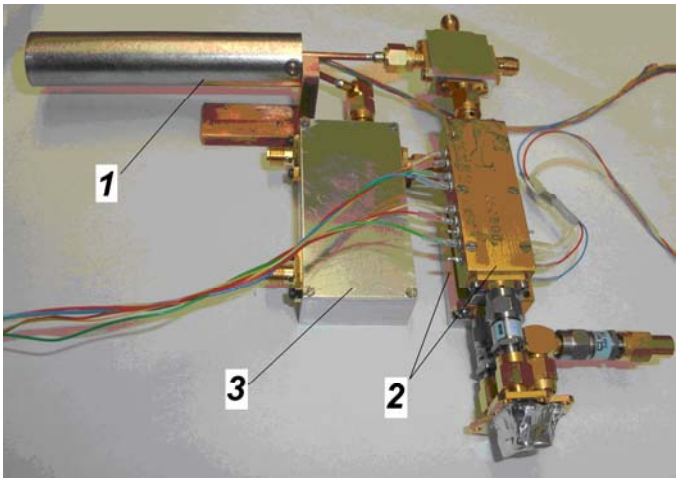

Fig. 3. Photo of the CPLL with operation frequency 4 GHz. All loop elements are presented: 1 - cylindrical cryoperm shield with the FFO and the HM inside, 2 – HEMT amplifiers, 3 - aluminum box, which contains the CPD and the loop filter. The loop length is 50 cm.

Down-converted spectra of the FFO phase-locked (PL) by different systems are presented in Fig. 4; spectrum of the free-running FFO is also shown for comparison. From this figure one can see that increasing of the PLL BW leads to extension of the frequency range, where phase noise of the PL FFO is lower than level for the free-running FFO. Increase of the phase-noise at higher offset from the carrier (for example, at offsets 35 - 40 MHz for the CPLL with BW 40 MHz) is typical for any PLL system. At these frequencies phase of the return signal is shifted on π due to delay in the loop and instead of noise suppression the phase noise level increase takes place; position of these peaks gives a possibility to estimate the PLL BW.

Reduction of the loop delay due to latest modifications results in increasing of the BW up to 40 MHz (Fig. 4 curve 2). For the FFO linewidth of 2 MHz this CPLL is able to phase-lock 94% against 82% for the RT PLL (Fig. 4a). For the FFO linewidth of 7 MHz the new CPLL gives SR = 81% instead of 41% for the RT PLL. Even more considerable gain was obtained at larger free-running FFO linewidth (see Fig. 5): SR = 63 % by the CPLL against 23 % for the RT PLL.

Summary of these results is presented in Fig. 6. Experimental data for the RT PLL with the BW of 12 MHz are shown by stars, for the CPLL with BW 25 MHz by squares and triangles show results for new CPLL with BW 40 MHz. Lines are results of numerical simulations [12] approximating the experiment. The "regulation BW" of 10 MHz in simulations corresponds to "BW" = 12 MHz in experiment. Data for new CPLL are approximated by a solid line (effective regulation BW 30 MHz in simulations); these data show the advantage of BW widening and prospects for future improvement. It can be approximately stated that twice wider FFO line can be phase locked by the PLL with two times wider BW resulting in the same SR.

It should be noted that total group delay for new CPLL should be 3 ns, but both the BW and the SR measurements indicate on the delay of about 4.5 ns. It means that additional delay of about 1.5 ns is still present in some elements of the loop; the origin for this delay is under investigation.

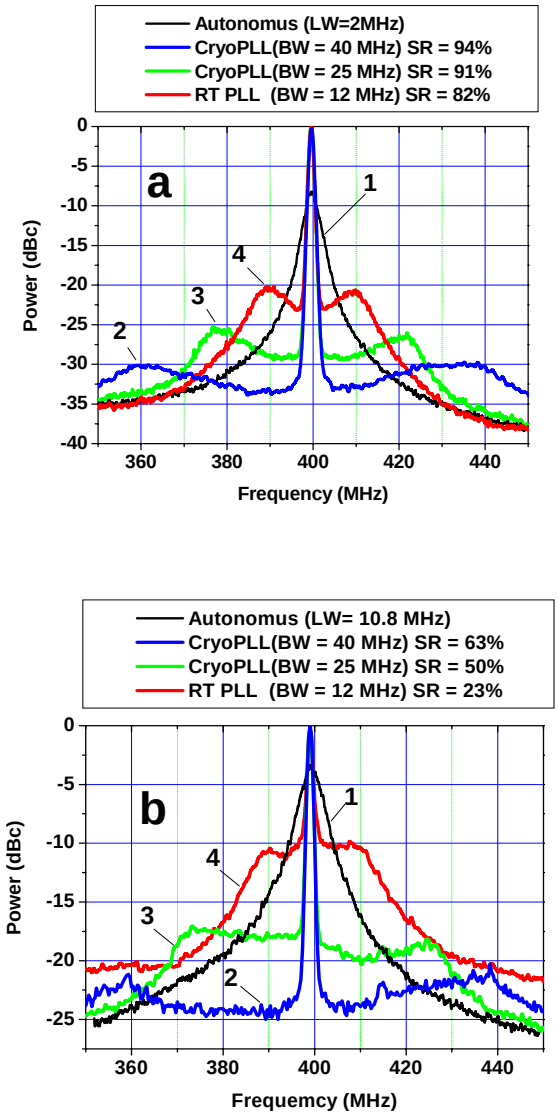

Fig.4. Down-converted spectra of the FFO operating at 600 GHz: curve "1" – autonomous, "2" – phase locked with CPLL (BW 40 MHz); "3" - phase locked with CPLL (BW 25 MHz) "4" – phase locked with RT PLL.

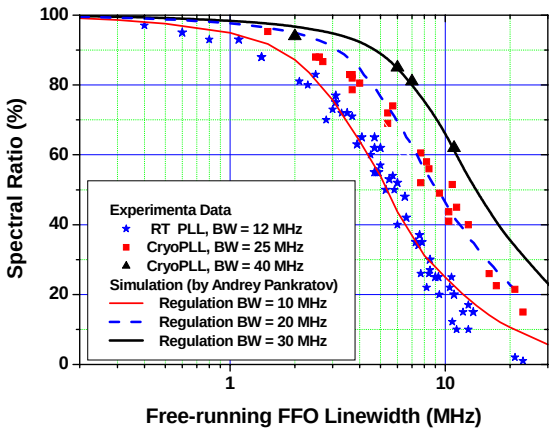

Fig. 5. Dependence of the SR vs FFO linewidth for different PLL bandwidths.

IV. Conclusion

Ultra wideband Cryogenic Phase Locking Loop system has been developed and tested. The CPLL has a bandwidth wider than 40 MHz and demonstrate an evident advantage on the RT PLL. The novel CPLL system can phase-lock more than 50% of the FFO spectral line if the free-running FFO is about 10 MHz. Practical implementation of CPLL looks especially promising for phase-locking of novel superconducting local oscillators utilizing NbN / NbTiN films, as well as for interferometry applications where extremely low LO phase noise is required.

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