Cryogenic Phase Locking Loop System for Superconducting Integrated Receiver

Andrey Khudchenko, Valery Koshelets, Pavel Dmitriev, Andrey Ermakov - *Institute of Radio Engineering and Electronics (IREE), Moscow, Russia*

Pavel Yagoubov - *SRON Netherlands Institute for SpaceResearch, the Netherlands*

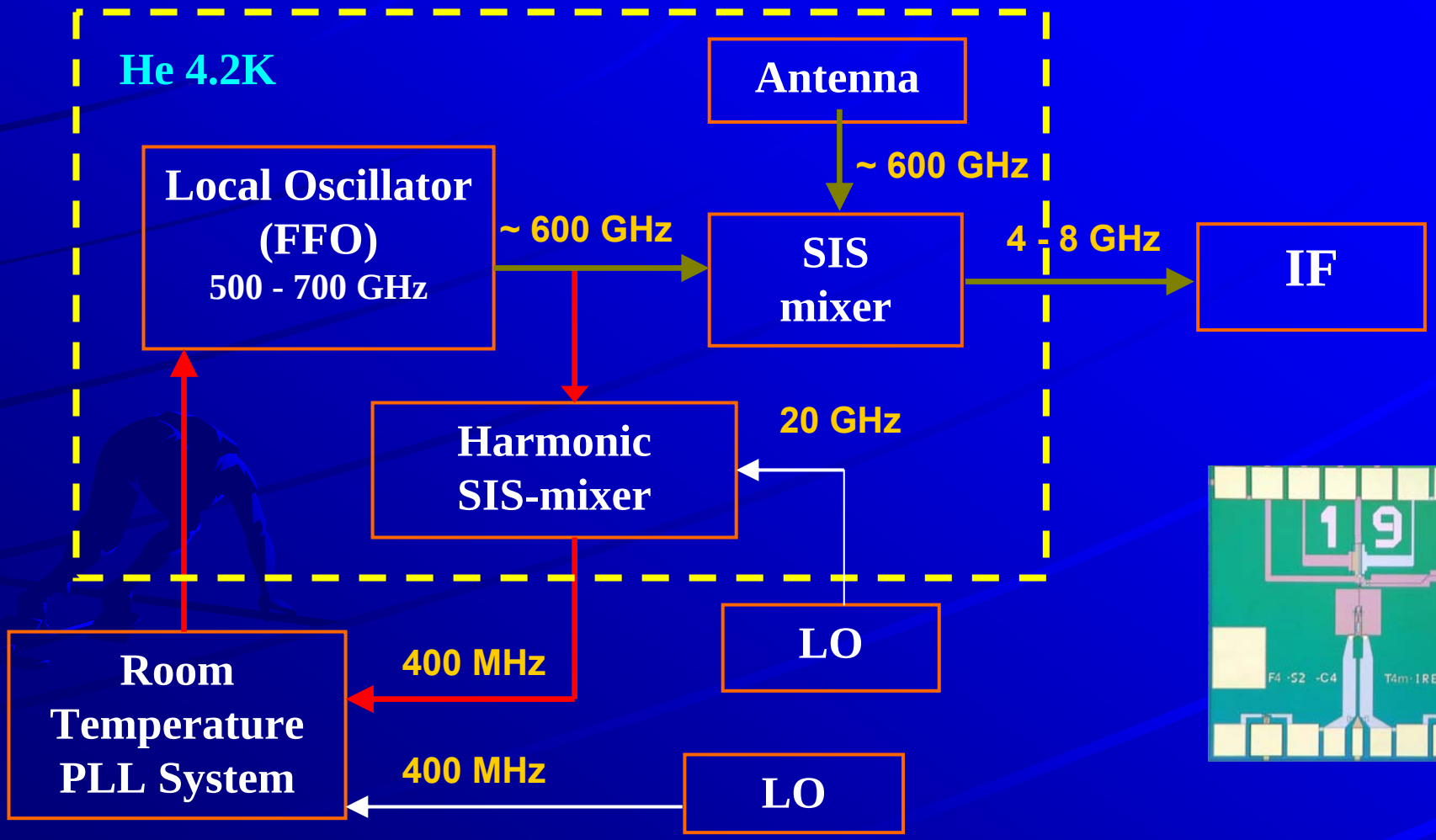
in collaboration with **Oleksandr Pylypenko** - *State Research Center of Superconducting Electronics "Iceberg", Kyiv, Ukraine*

Cryogenic Phase Locking Loop System for Superconducting Integrated Receiver

Outline

- Introduction - Superconducting Integrated Receiver (SIR)
- FFO Phase Locking – performance and prospects
- SIS-junction as a Cryogenic Phase Detector (CPD)
- CPD and FFO coupling
- Cryogenic Phase Lock Loop system - experimental results
- Conclusion

Block Diagram of Superconducting Integrated Receiver



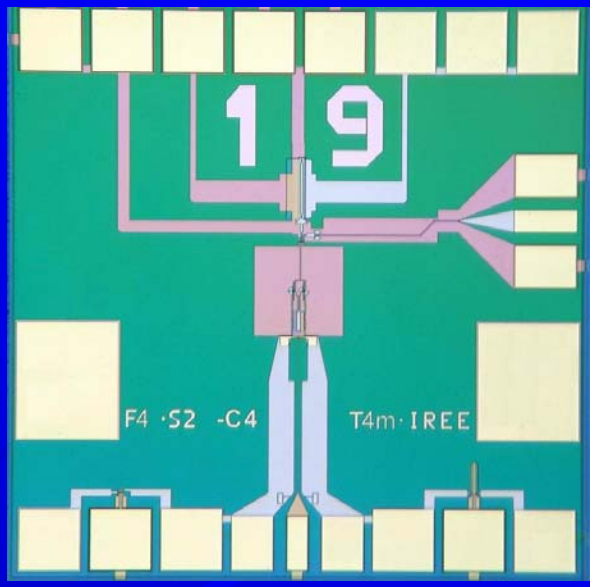
Superconducting Integrated Receiver (SIR)

APPLICATIONS

- **Airborne Receiver for Atmospheric Research and Environmental Monitoring; Radio Astronomy;**
  Large Imaging Array Receiver
  Laboratory MM & subMM Spectrometer

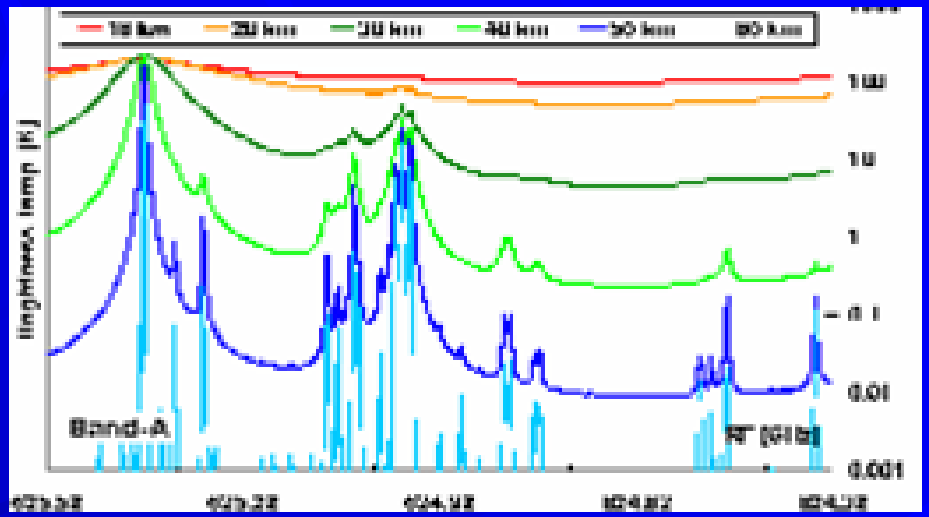
STATE OF THE ART

- **Single chip Nb-AlOx-Nb SIS receivers with superconducting FFO has been studied at frequencies from 100 to 700 GHz**
- **A DSB receiver noise temperature as low as 90 K has been achieved at 500 GHz**
- **9-pixel Imaging Array Receiver has been successfully tested**
- **Phase Locked operation from 550 to 700 GHz**
- **TELIS - balloon-borne spectrometer, the qualification flight is foreseen in May 2008**

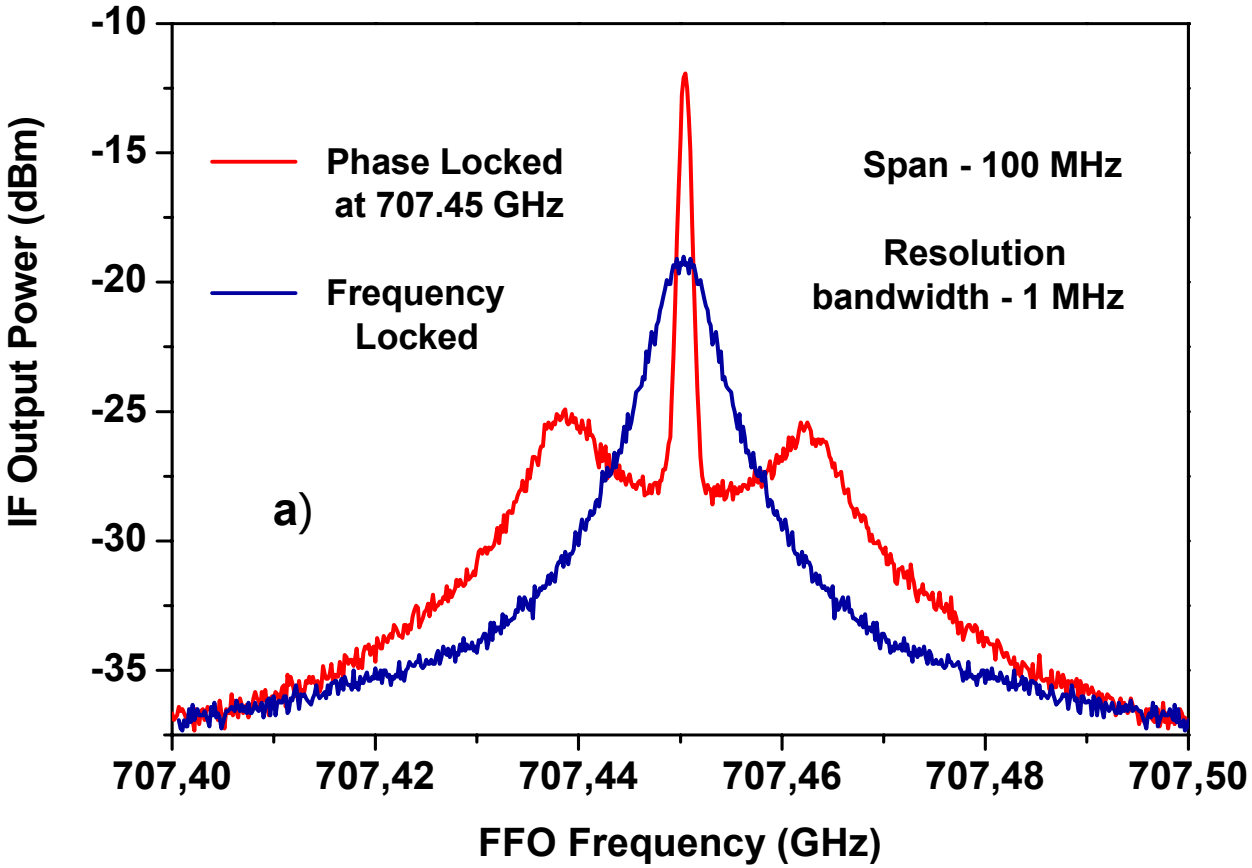


SIR FFO prospects

- For future SIR applications (f>1THz) FFO with NbN electrodes will be used; FFO linewidth could considerably exceed 10 MHz.
  So ultrawideband PLL is required (>30 MHz).
- Cryogenic PLL with small power consumption for large SIR arrays

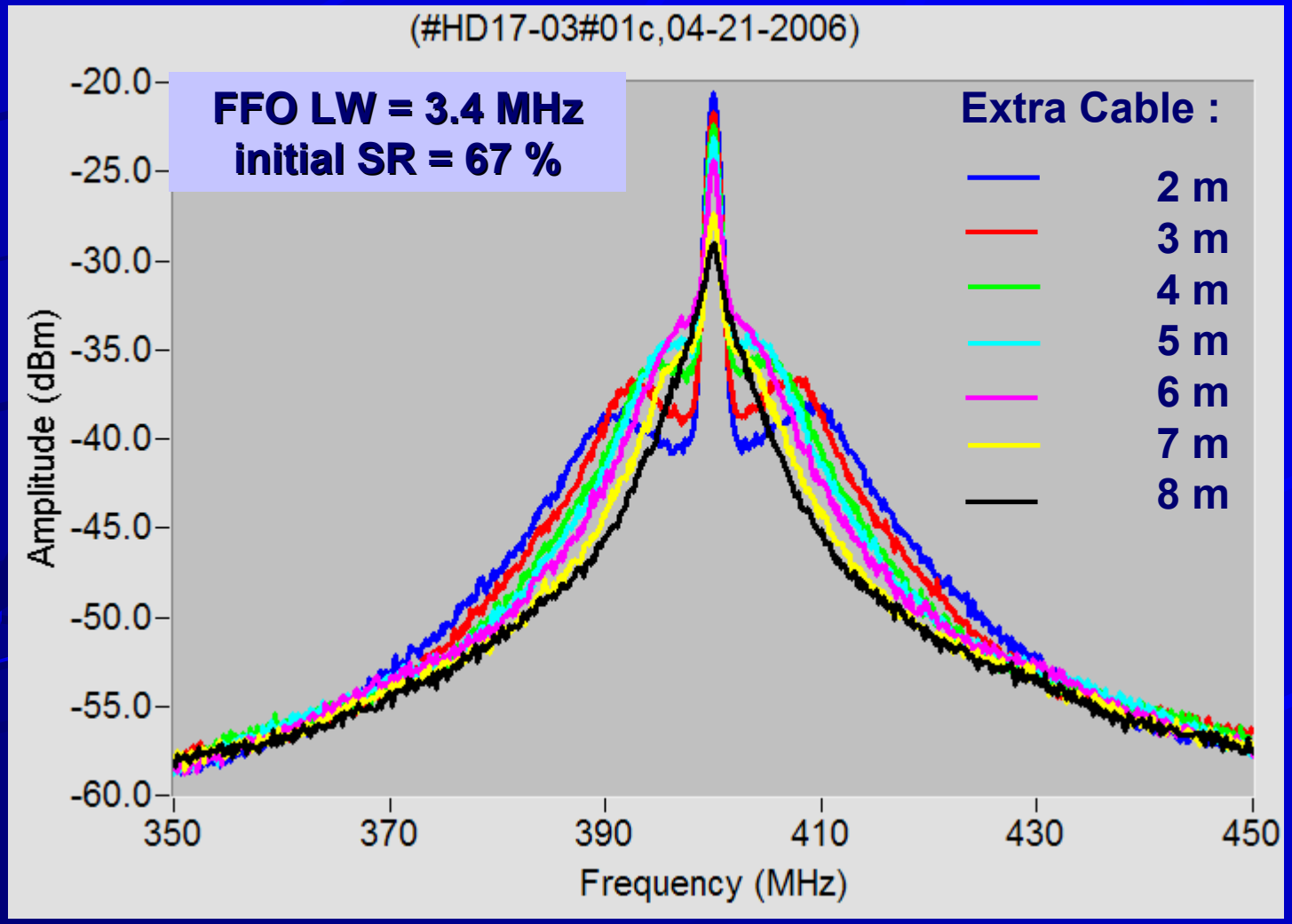


Spectra of the FFO at 707.45 GHz

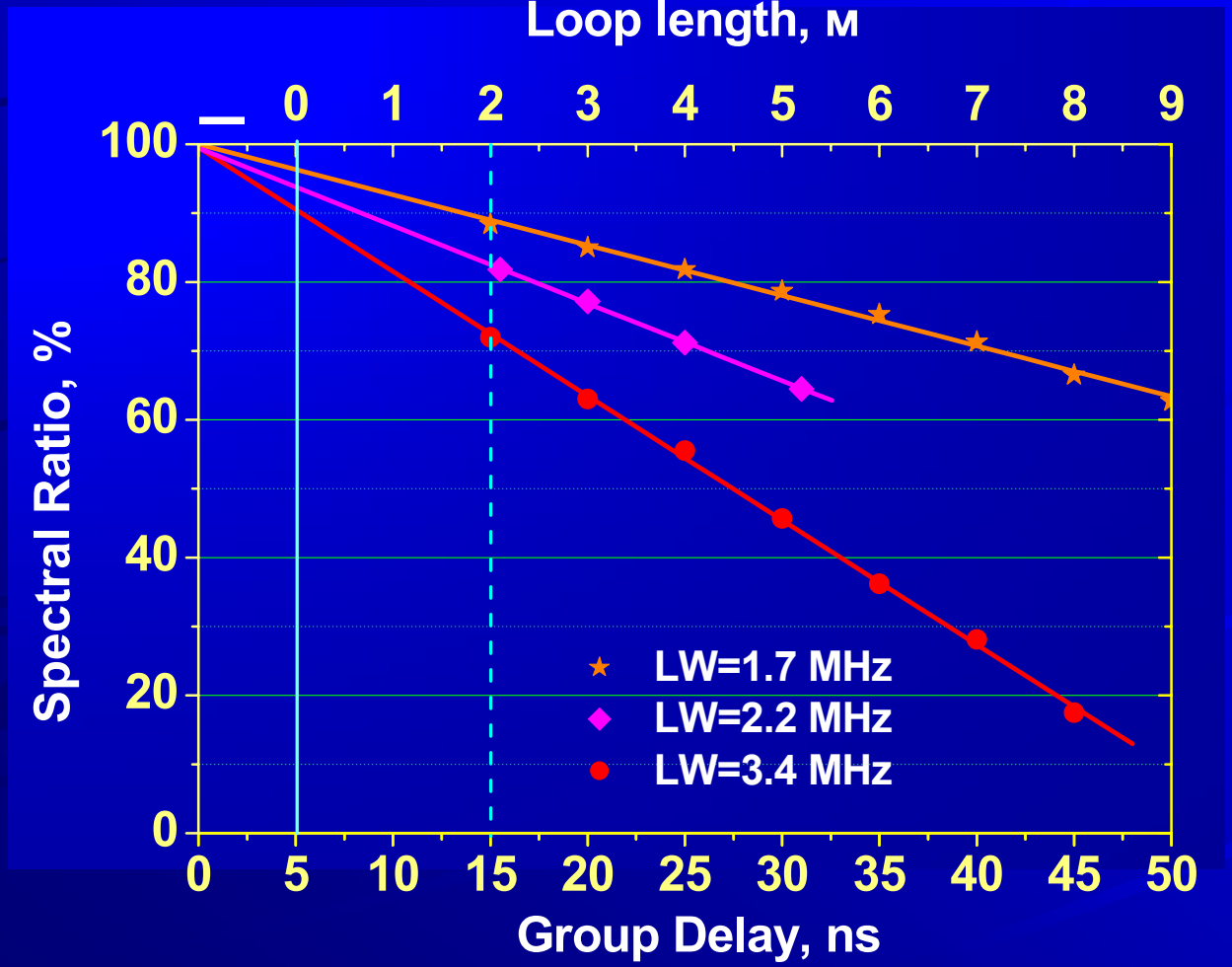


Spectral Ratio (SR) – the part of FFO power locked by PLL system

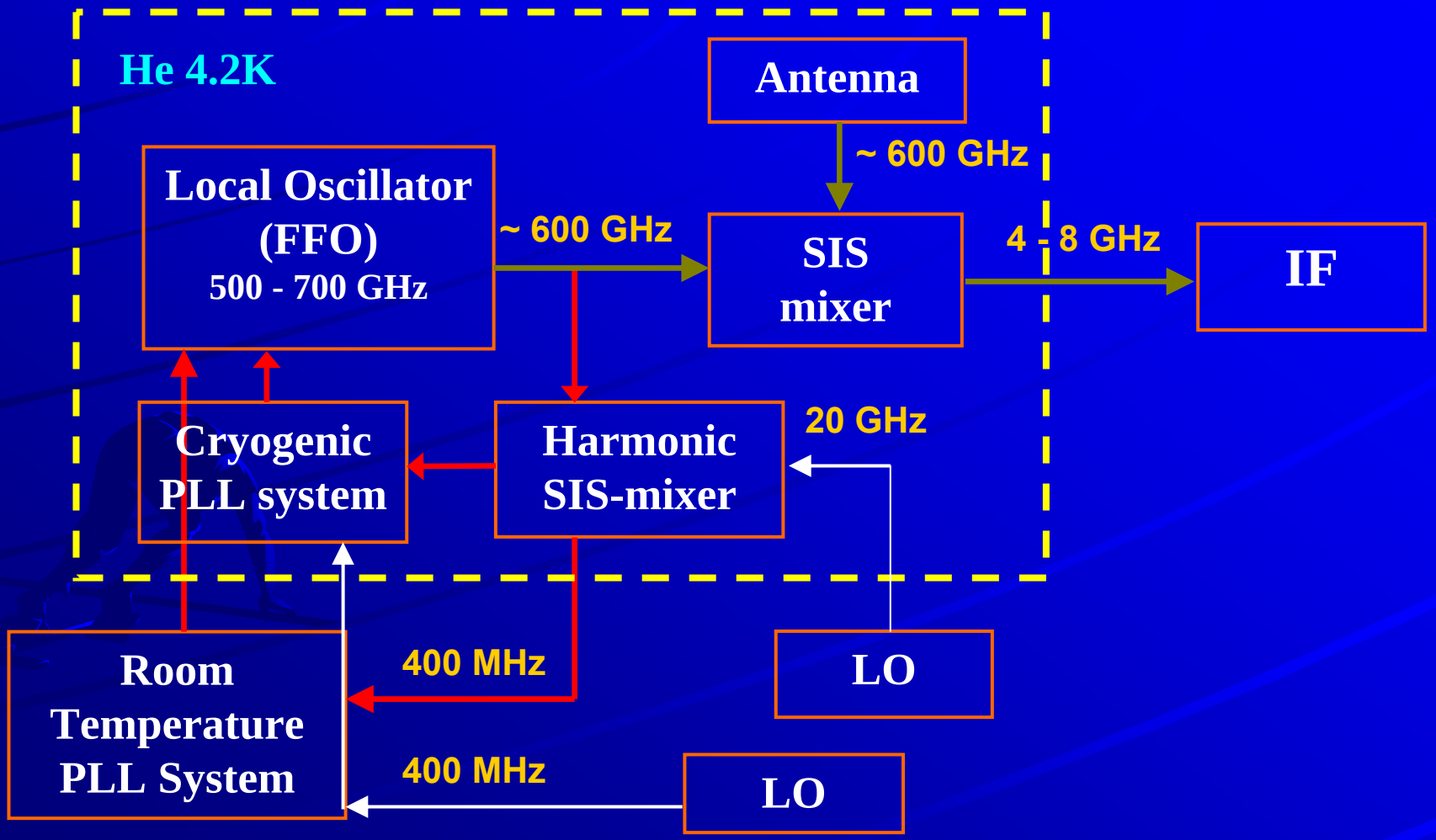
Spectra of the phase-locked FFO for different delay in the PL loop



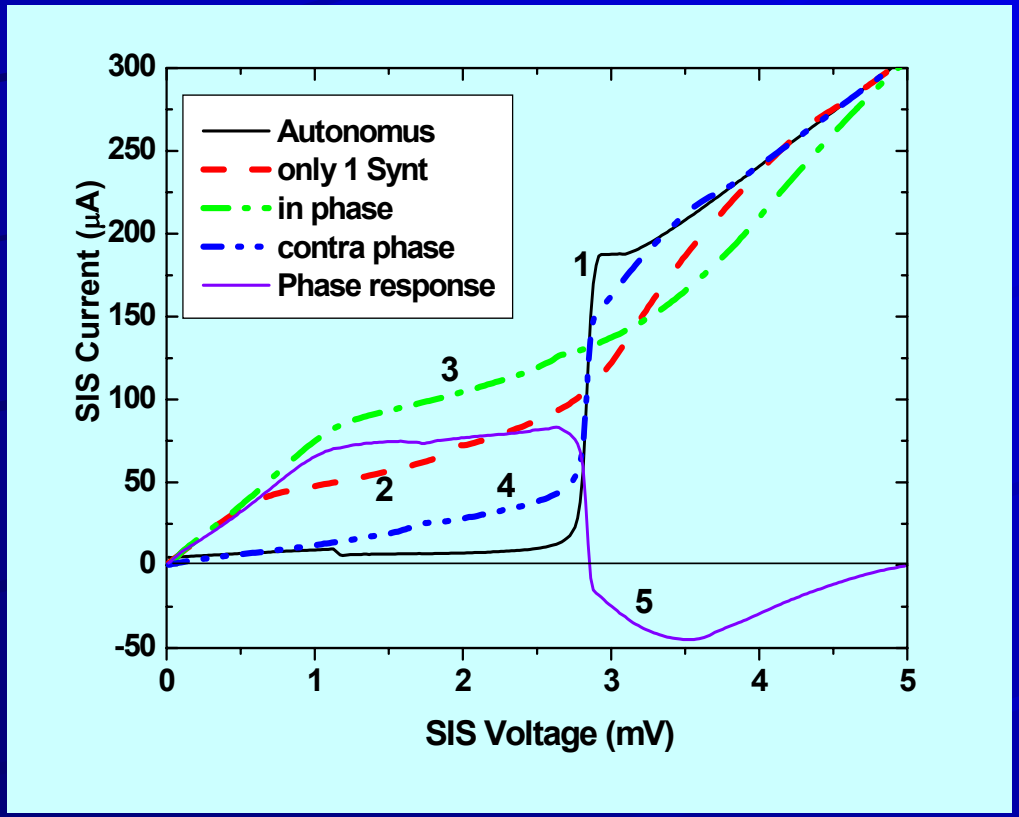
SR value on the delay in PL loop

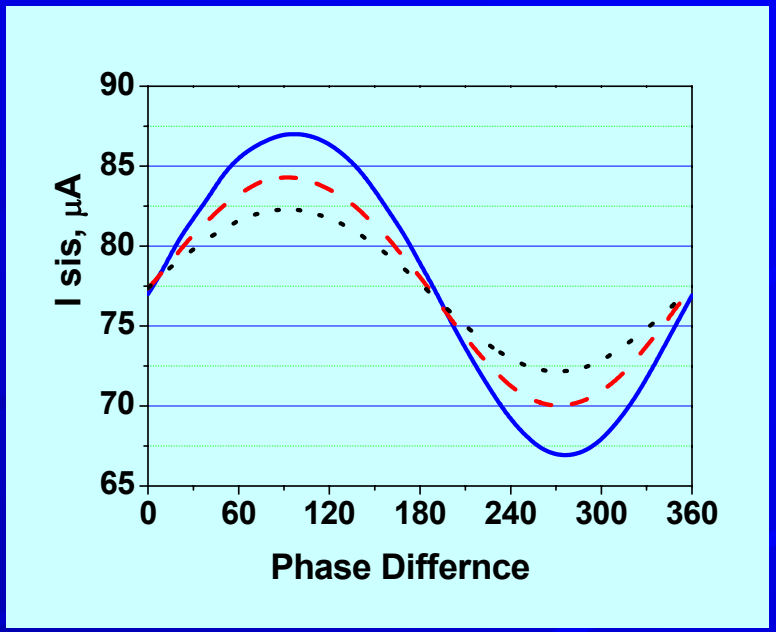


Idea of the Cryogenic Phase Lock Loop System

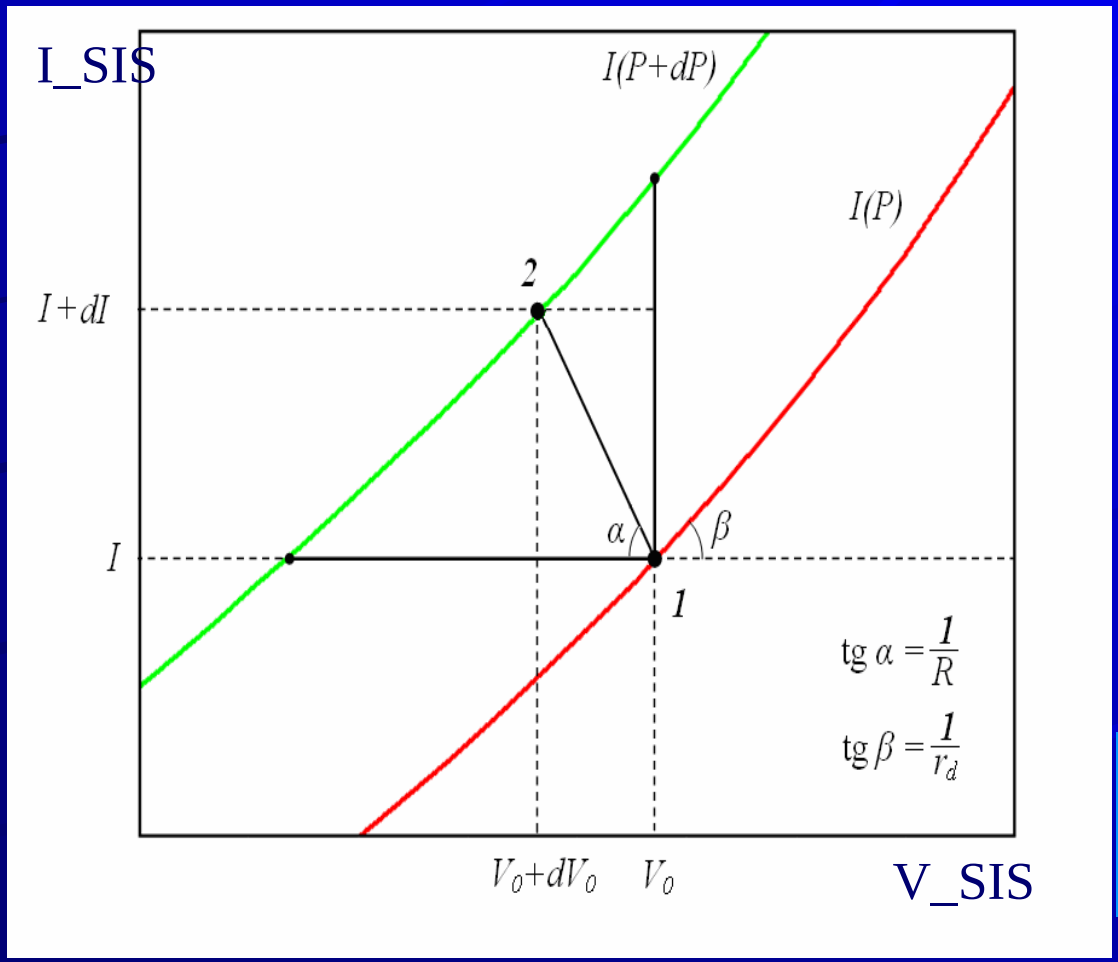


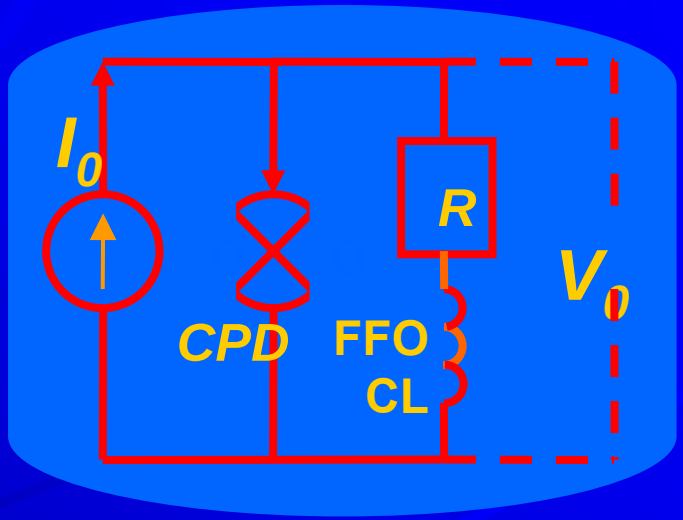
SIS-junction as a Cryogenic Phase Detector





CPD and FFO coupling

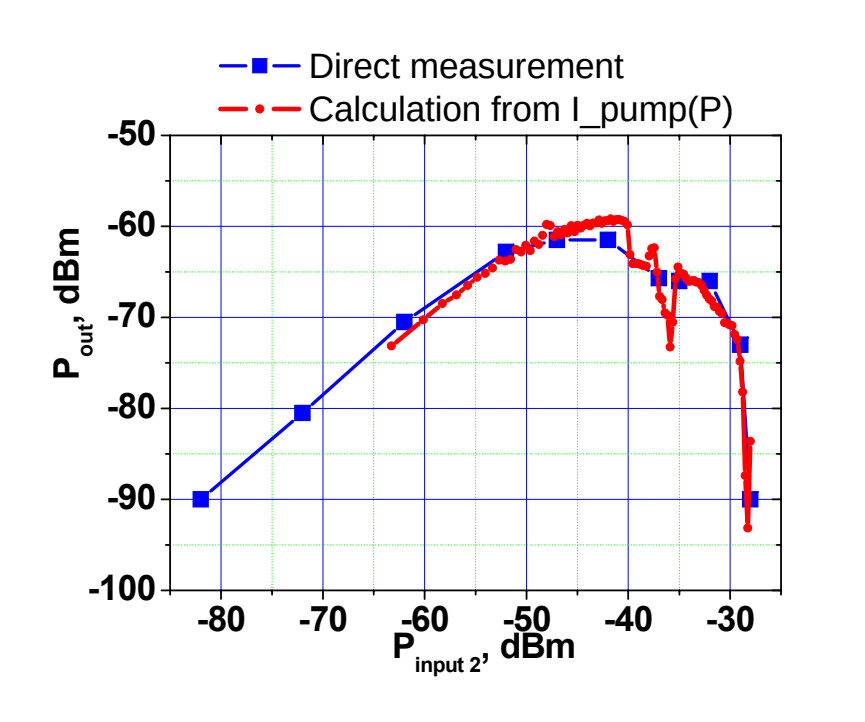


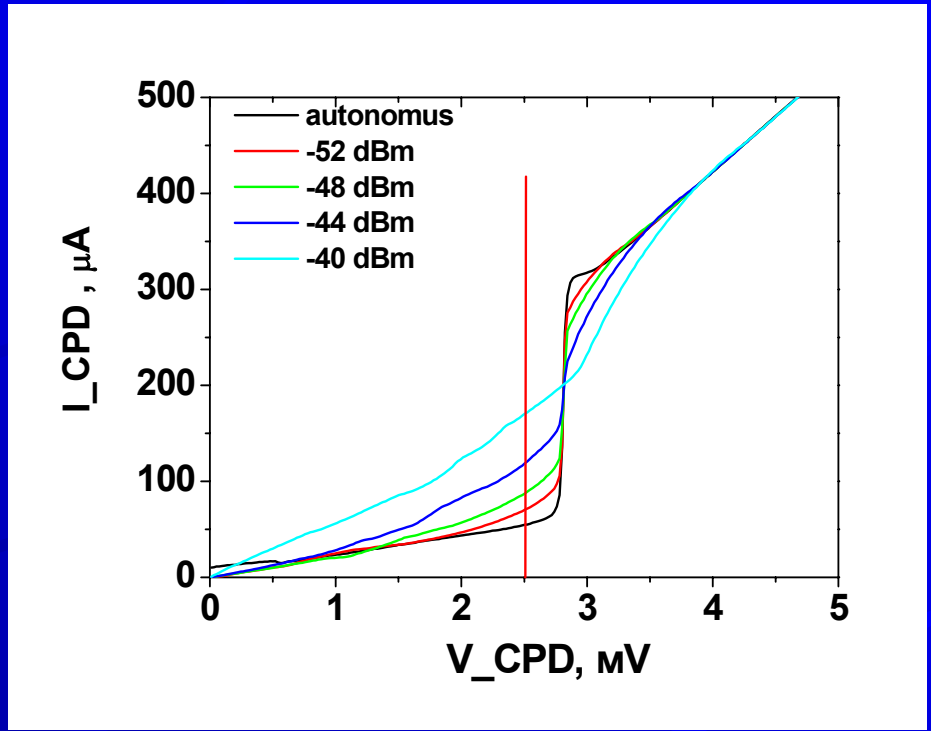


r_d - CPD differential resistance

$$dI_{CL\_FFO} = -\frac{r_d}{r_d + R} \cdot \frac{\partial I_{CPD}}{\partial P} dP$$

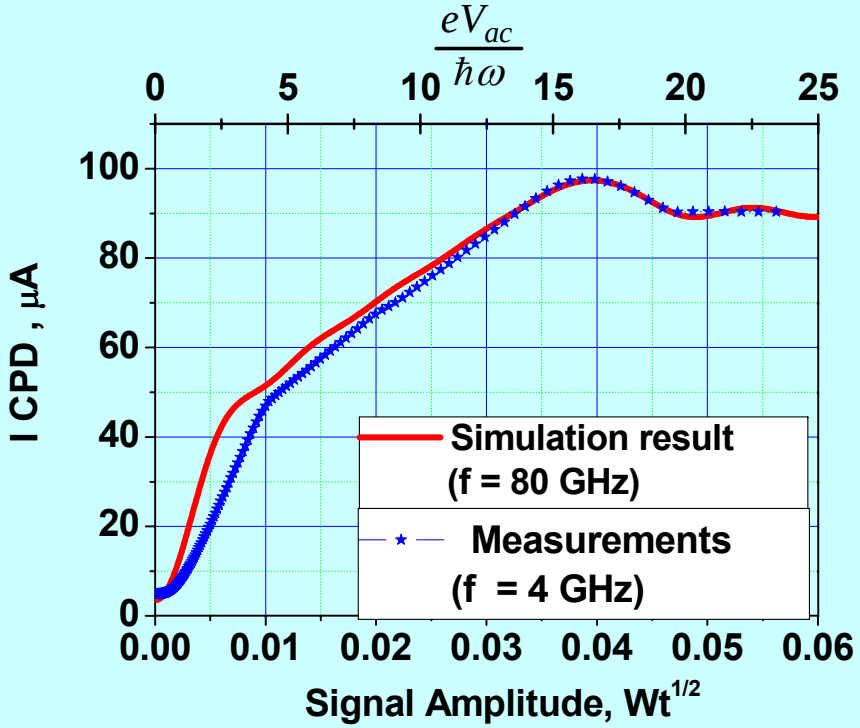
CPD output, I_pump(P)

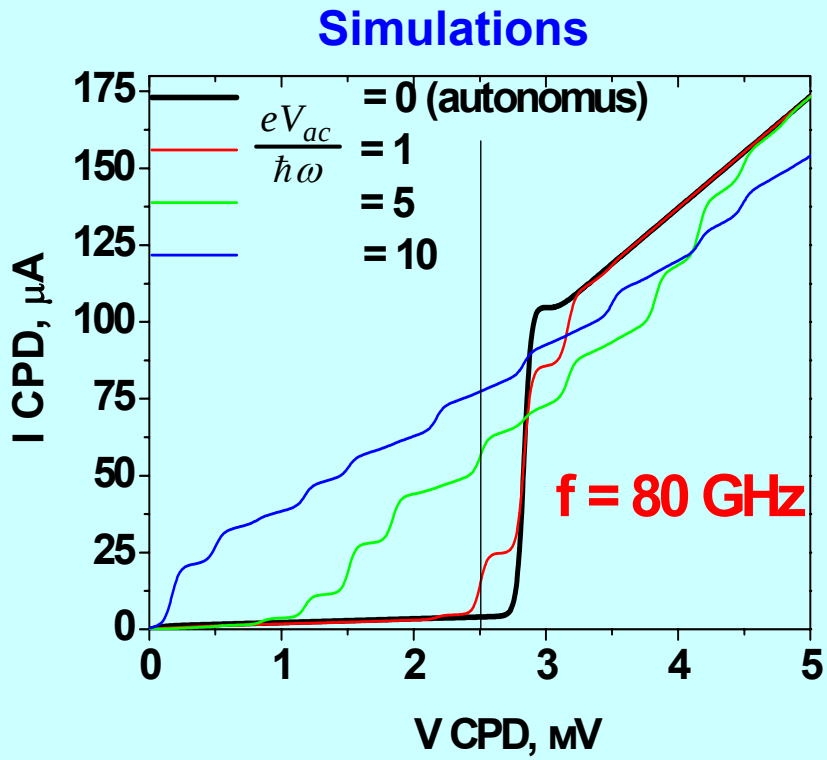




P_pump(P) model

$$I(V_{dc},\omega,V_{ac}) = \sum_{n=-\infty}^{+\infty} J_n^2\left(\frac{eV_{ac}}{\hbar\omega}\right) I_0\left(V_{dc} + \frac{n\hbar\omega}{e}\right)$$





CryoPLL Block diagram

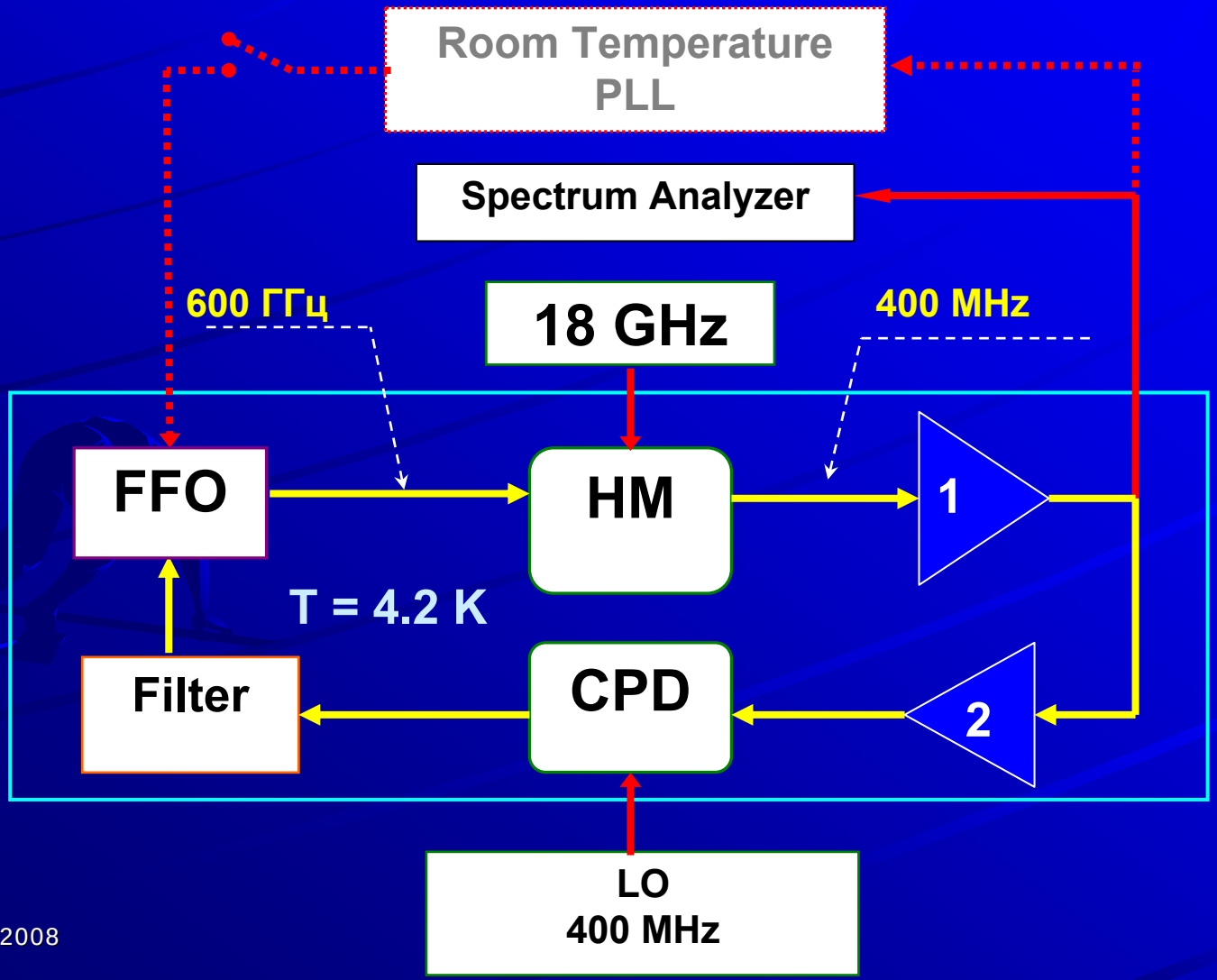
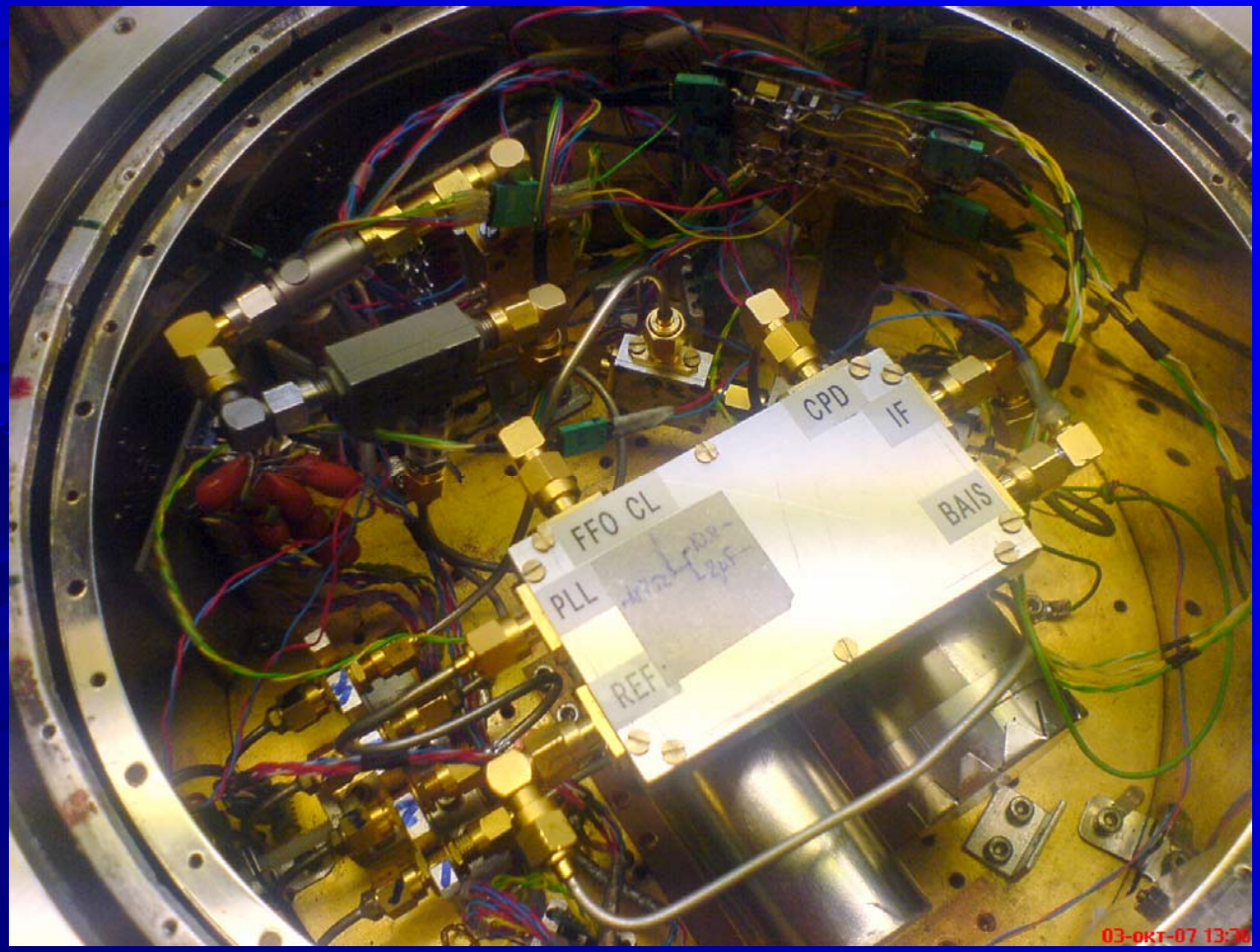
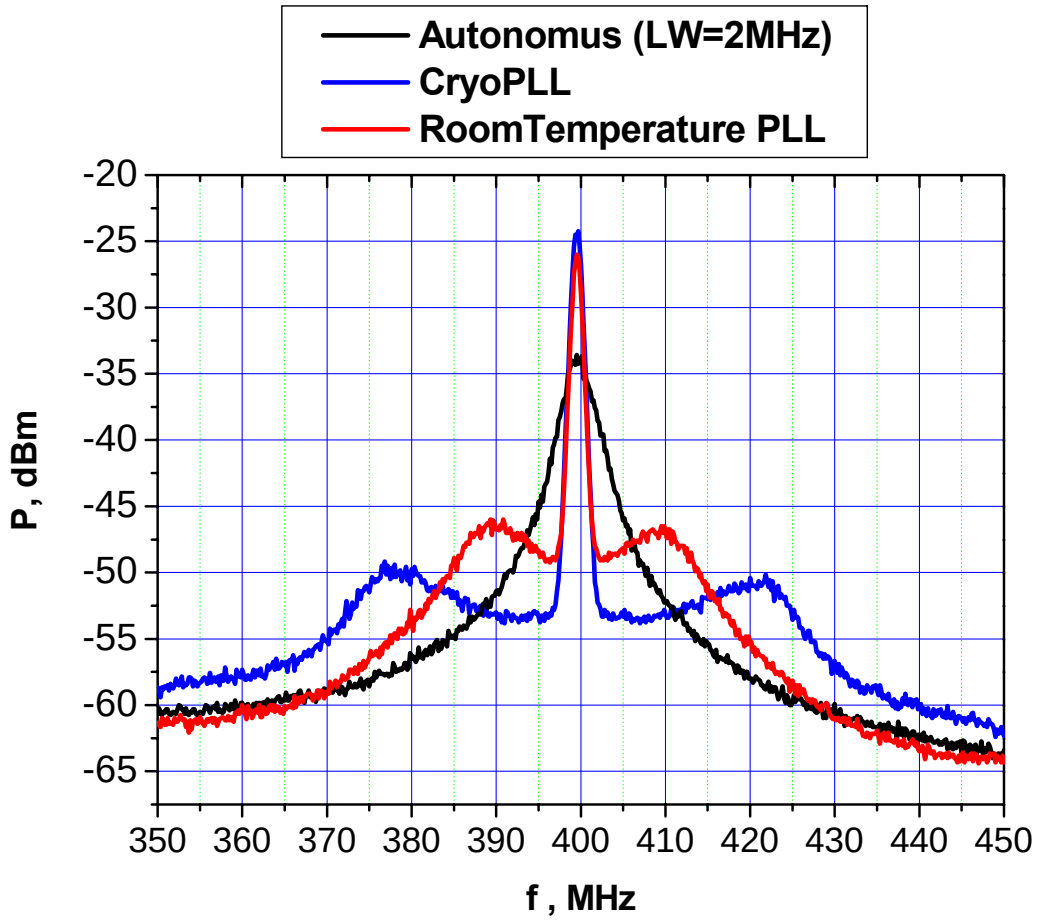


Photo of the CryoPLL

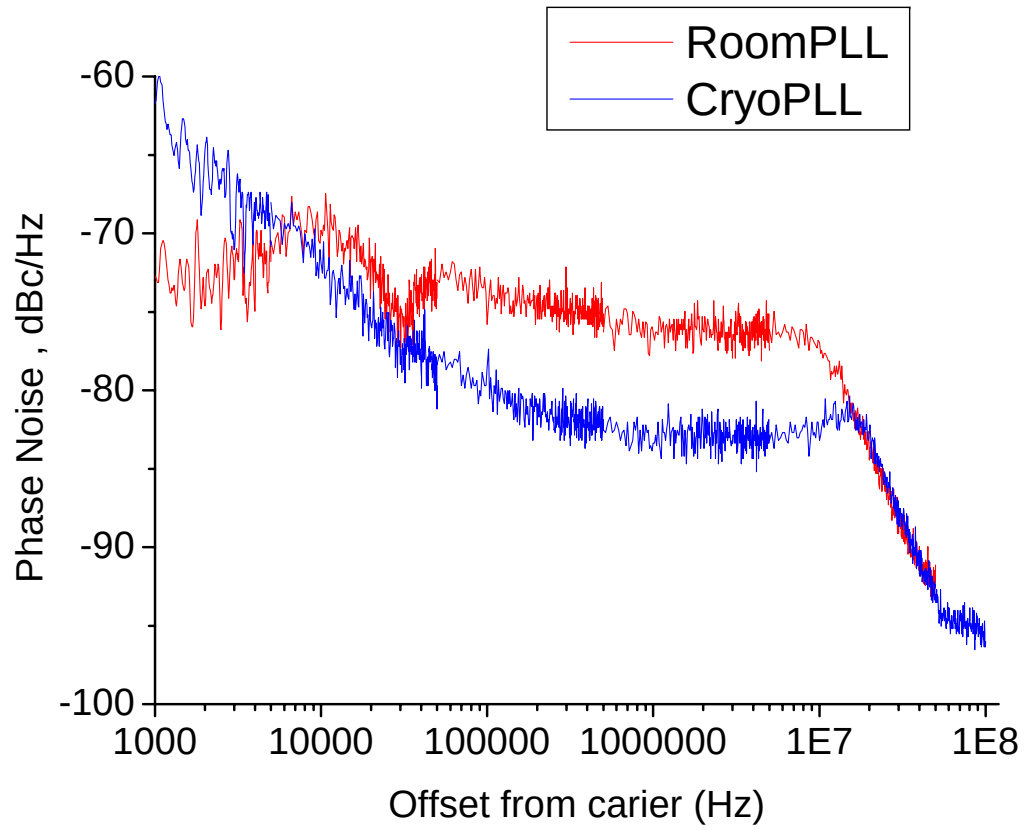


Spectra of PLL and CryoPLL



	CryoPLL	RoomPLL
Loop length, м:	1	2
Delay in elements, ns:	2	5
Total Delay, ns:	7	15
Bandwidth, MHz	27	12
SR, % (for LW=2 MHz)	91	82

Phase Noise



For FFO Linewidth
9 MHz
PLL gives SR = 25%
_CryoPLL - 53%!

Conclusion

- New and successful application of SIS junction - cryogenic phase detector (CPD).
- CPD intrinsically could operate with effective bandwidth more than 100 MHz. Maximal output signal is about 0.1 mV.
- Concept of CryoPLL system is confirmed. Bandwidth 27 MHz has been obtained in the first experiments.
- Improvement of the PLL FFO spectral ration from 20% to 50% has been achieved at application of the CryoPLL for FFO linewidth 10 MHz.
- Practical application of the CPD looks especially promising for the development of SIR arrays.