Cryogenic Phase Detector for Superconducting Integrated Receiver

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Abstract—New superconducting element, a cryogenic phase detector (CPD) has been proposed and preliminary tested. The CPD is based on a superconductor-insulator-superconductor junction and initially intended for phase locking of a flux-flow oscillator in a superconducting integrated receiver. First results of the CPD development and study are very encouraging; a sinusoidal response of the CPD has been measured at the variation of the phase shift between input signals. Dependences of the output signal and phase response on the CPD bias voltage have been studied; main parameters of this new device are estimated. Important that the CPD output current well above 10 μA has been measured at the input signal provided by the harmonic mixer of the integrated receiver and amplified by the existing HEMT-amplifier. Due to the large conversion coefficient this current being supplied to the flux-flow oscillator (FFO) control line is sufficient to directly tune FFO frequency. Obtained data demonstrate that the CPD intrinsically could operate with effective bandwidth more than 100 MHz. Preliminary results of the CPD implementation for the FFO phase locking are presented; possible advantages of such combination are discussed.

Index Terms—Phase detection, superconducting integrated circuits, superconductor-insulator-superconductor devices.

I. INTRODUCTION

RECENTLY a concept of the Superconducting Integrated Receiver (SIR) has been proposed and successfully proven [1], [2]. The SIR comprises in one chip a planar antenna integrated with a superconductor-insulator-superconductor (SIS) mixer, a superconducting flux flow oscillator (FFO) acting as Local Oscillator (LO) and a second SIS harmonic mixer (HM) for FFO phase locking. Detailed measurements of the FFO linewidth [3] demonstrate Lorentzian shape of the FFO line in a wide frequency range up to 700 GHz. It means that the free-running ("natural") FFO linewidth is determined by the wideband thermal fluctuations and the shot noise. This is different from many traditional microwave oscillators where
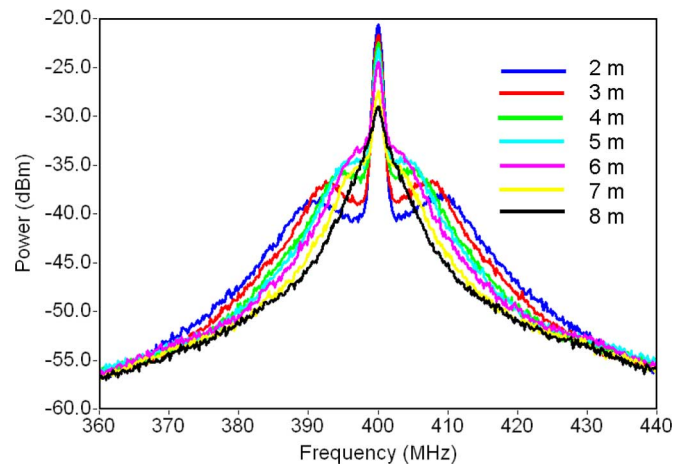
Fig. 1. Spectra of the phase-locked FFO (FFO frequency 648 GHz; free-running linewidth 3.4 MHz; initial $SR = 67\%$), measured at different length of the PL loop (extra cable was added with increment 1 m between PLL output and cryostat).

the "natural" linewidth is very small and is smeared mainly by external fluctuations. That is why for stabilization of the FFO frequency a specially designed wide-band phase lock loop (PLL) system is required; the effective bandwidth of the existing room temperature PLL system is about 10 MHz.

Since the free-running FFO linewidth may be as large as 10 MHz (at some specific FFO frequencies [4] due to Josephson self-coupling effect) only limited part of the emitted by the FFO power can be phase-locked by room temperature PLL system. For example, the ratio between the locked by PLL (carrier) and the total power emitted by the FFO—so called spectral ratio (SR)—for the present PLL system is only about 50% at a free-running FFO linewidth of 7 MHz. To overcome this limitation we propose a cryogenic phase detector (CPD) based on a well-developed tunnel SIS junction. Such CPD would have minimal internal delays and could be placed very close to the FFO.

II. PHASE LOCKING OF THE FLUX FLOW OSCILLATOR

The effective bandwidth of the existing PLL system used for the FFO phase locking is limited by the signal delay in the PLL and (mainly) by the delay in the cables between cryogenic FFO and room temperature PLL electronics. Importance of the PLL cables length for the PL FFO performance is illustrated in Fig. 1 (note that minimal possible length of the cables in the regular PLL system used for the FFO LW measurements is about 2 m—mainly length of the cables inside the cryostat).

It was found experimentally that in the wide range of parameters the SR of the phase-locked FFO varies linearly with the
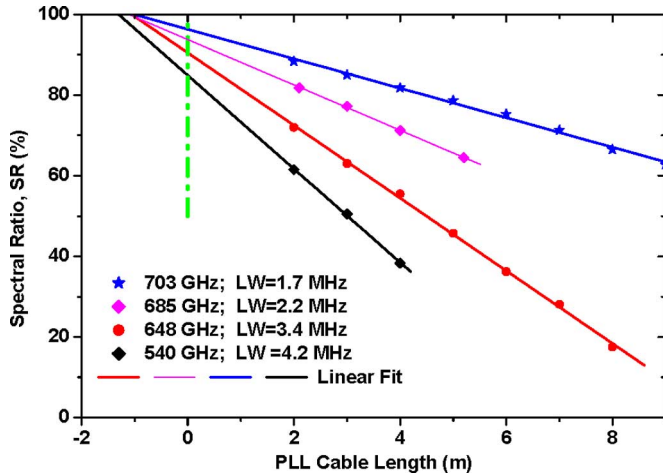
Fig. 2. Dependence of the SR value on the length of the extra cable added to the PL loop for two different FFO frequencies.

Fig. 3. IVCs of the SIS junction measured at different settings of the synthesizers (frequency 5 GHz): curve "1"—autonomous ($PSynth1 = PSynth2 = 0$); "2"—pumped by one synthesizer ($PSynth1 = 0.3\ \mu W$, $PSynth2 = 0$); "3"—pumped by 2 synthesizers in phase ($PSynth1 = 0.3\ \mu W$, $PSynt2 = 0.1\ \mu W$, phase difference $= 0$); "4"—pumped by 2 synthesizers in anti-phase ($PSynth1 = 0.3\ \mu W$, $PSynt2 = 0.1\ \mu W$, phase difference $= 180$); "5"—phase response of the CPD—difference between curves "3" (in phase) and "4" (antiphase).

length of the phase-lock loop (see Fig. 2). Slope of the lines depends monotonically on the free-running FFO LW; furthermore, the point of intersection of all these curves lays on the horizontal line corresponding to $SR = 100\%$ (in the point where the cable length is formally about -1 m). The region of the graph left to the dashed line (which marks a "zero length limit") corresponds to a delay introduced by the PLL system itself. From Fig. 2 one can see that this value is about 1 m (that corresponds to the delay of 5 ns; it gives consequently the intrinsic PLL regulation bandwidth of the order 50 MHz). For wide enough initial FFO linewidth $(LW > 4\ MHz)$ the point of intersection moves to the left. It might be explained by the reduction of the effective PLL regulation bandwidth, since the ultimate PLL regulation bandwidth can't be realized for very wide FFO linewidth presumably due to decreased S/N ratio of the IF signal at the PLL input.

A considerable reducing of the delays in the PLL system and in the PLL cables would give a possibility to phase lock much more FFO power compared to regular room-temperature PLL systems. To realize this goal, a PLL system with negligibly small internal delay should be placed near the FFO to minimize the cable length. Traditional semiconductor PLL system will not operate at low temperature inside a cryostat. Moreover, to provide a large enough input signal needed for its operation, the total gain of the IF amplifier of about 100 dB is required (that is unacceptable inside a cryostat due to possible chain excitation). Proposed CPD could be placed very close to the FFO and does not require very large input signal.

III. EXPERIMENTAL RESULTS

A. Experimental Details

For the first try as a CPD we used micron size Nb-AlOx-Nb tunnel junctions originally fabricated as a part of the integrated circuit for FFO linewidth measurements. This junction was designed as a harmonic mixer with appropriate tuning circuits that tune SIS capacitance at frequencies 400–700 GHz; for these experiments only HM was biased while no biasing was applied to the FFO. Devices from different batches were tested;
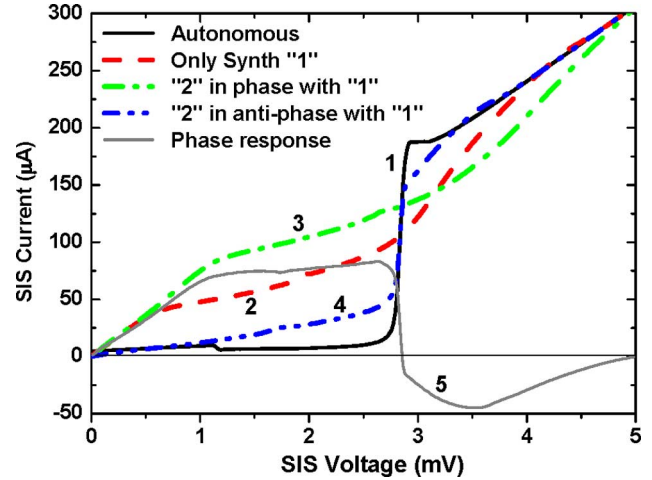
obtained results are similar for all these samples. Signals from 2 synthesizers are combined together and applied to the SIS via directional coupler; DC and IF output of the SIS respectively can be continuously measured by data acquisition system and monitored by spectrum analyzer. It should be noted that we performed measurements at different frequencies: from 0.5 up to 5 GHz; all results were qualitatively quite similar.

The results presented in this report were obtained with suppressed SIS junction critical current. The presence of a critical current considerably modifies I-V curves of the SIS junction due to Josephson effect. However our measurements demonstrated that there is no significant influence of the critical current on the phase response.

B. Demonstration of CPD Operation

Typical autonomous IVC of the SIS junction is presented in Fig. 3 by curve 1; IVC of the SIS pumped by one synthesizer is shown by curve 2. Although the frequency of the synthesizer is rather low (compared to the energy gap smearing); the pumped IVC resembles result of high frequency irradiation rather than noise suppression that one can expect at application of low frequency signal to tunnel junction. Presumably high harmonics of the applied signal are excited in the SIS junction due to its non-linearity; these high frequency harmonics effectively pump the tunnel junction.

Curves 3 and 4 show results of the joint action of two synthesizers: for curve 3 the synthesizers are in phase, for curve 4—in anti-phase (180 degree shift). The difference between curves 3 and 4 (phase response) is also presented in Fig. 3. Note that at the typical value of the FFO $R_{dCL} = 0.02\ Ohm$ the output current 50 μA would produce the FFO frequency shift of 500 MHz. The output current of the phase detector is large enough to drive directly the FFO although a possibility of direct connection of the CPD and the FFO should be checked experimentally. It is important also that there is quite large
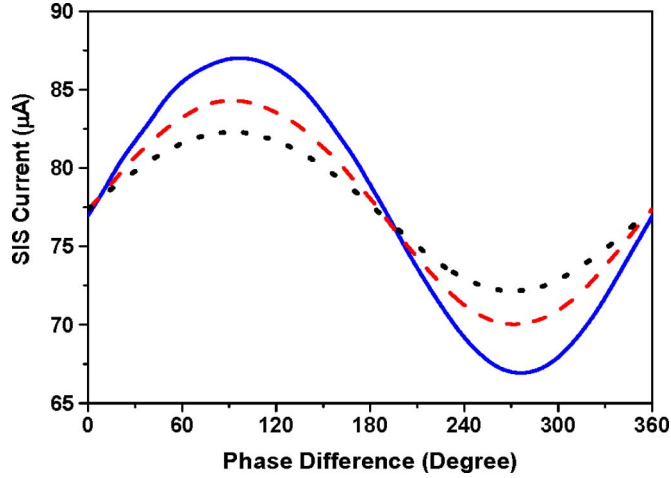
Fig. 4. Dependence of the SIS current on the phase difference between the signals. Three cases for different powers of one of the synthesizers are presented. $f = 4\,\mathrm{GHz}$; $\mathrm{Vsis} = 2.55\,\mathrm{mV}$.
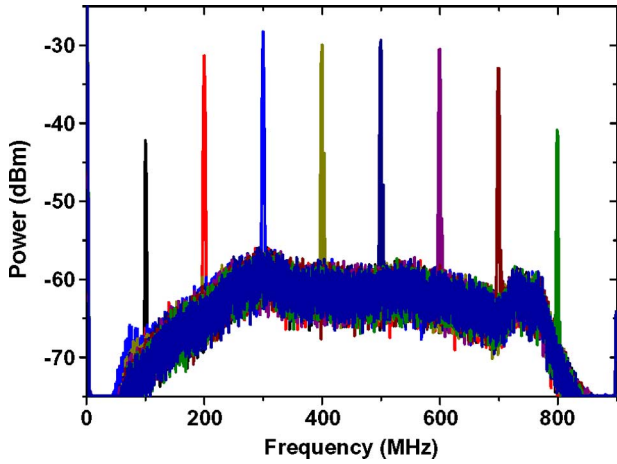

Fig. 6. SIS current versus amplitude of the microwave signal ($f = 4\,\mathrm{GHz}$, $\mathrm{Vsis} = 2.55\,\mathrm{mV}$).

All results presented in this section demonstrate that a SIS junction can be used as a phase detector that is able to operate with an internal delay <1 ns and can be placed directly near the FFO to control its phase.

C. Power Issue; Experimental Results and Analysis

A total power P applied to the SIS is a coherent combination of incident signals:

$$P = P1 + P2 + 2\sqrt{P1P2}\cos\varphi, \qquad (1)$$

where P1 is power of the synthesizer 1, P2—power of the synthesizer 2, φ—the phase difference between these two signals. The amplitude for two important cases can be written: $\sqrt{P(\varphi = 0)} = \sqrt{P1} + \sqrt{P2}$ (in-phase signals) and $\sqrt{P(\varphi = 180°}} = \sqrt{P1} - \sqrt{P2}$ (anti-phase signal). In the amplitude representation the summary signal oscillates around $\sqrt{P1}$ with the amplitude $\sqrt{P2}$ (for $P_2 \leq P_1$); therefore the phase response can be easily determined if the dependence of the SIS current on $\sqrt{P}$ is known.

Experimental dependencies $\mathrm{I_{SIS}}(P)$ were measured and corresponding curves $\mathrm{Isis}(\sqrt{P})$ were calculated; the typical dependence is presented in Fig. 6. There are two ranges of the $\sqrt{P}$ where this dependence is linear with a constant slope; we suppose that this behavior is related to the mixing properties of the SIS junction and to its interaction with the tuning circuitry.

Fig. 5. High-frequency output from the CPD. $\mathrm{P_{synt1}} = -27\,\mathrm{dBm}$, $\mathrm{f_{synt1}} = 5\,\mathrm{GHz}$; $\mathrm{P_{synt2}} = -60\,\mathrm{dBm}$, $\mathrm{f_{synt2}} = 5.0\ldots5.9\,\mathrm{GHz}$; $\mathrm{Vsis} = 2.6\,\mathrm{mV}$.

D. First Results of the FFO Phase Locking by CPD

A block diagram of the setup for demonstration of the CPD operation is shown in Fig. 7. The FFO frequency is about 600 GHz. The signal coming from the FFO is mixed in the SIS with the nth harmonic of the external synthesizer frequency 18 GHz. The intermediate frequency signal of about 400 MHz is amplified by the HEMT amplifier 1. After the splitting one part of the signal goes to the room temperature PLL system while second part is applied to the HEMT amplifier 2 with adjustable gain and then entered the CPD. So cryogenic and room temperature PLLs are connected in parallel. A small fraction of the signal is applied via the directional coupler to a spectrum analyzer. All the synthesizers and the spectrum analyzer are phase locked to a

range of the CPD bias where the phase response is almost independent on voltage (see Fig. 3).

At the proper setting of the experimental parameters the dependence of the phase response (PhR) is sinusoidal on the phase difference between two synthesizers (see Fig. 4). If the frequencies of the synthesizers are slightly different (f1 and f2 correspondingly), the beating between these frequencies takes place. This beating with the frequency f1–f2 can be measured directly by measuring the HM current at DC with appropriate filters setting.

If a difference between the synthesizer's frequencies is large, the CPD output signal can be amplified and recorded by the spectrum analyzer using standard HM IF chain employed for the FFO LW measurements. The results are presented in Fig. 5; in this case the difference between frequencies is going from 0 up to 900 MHz with a step 100 MHz. From this figure one can see that the frequency of the output signal is equal to the difference between the synthesizer's frequencies. Amplitude of the output signal is almost independent on the frequency difference (peaks of the output signal just follow the amplifier amplitude-frequency characteristics).
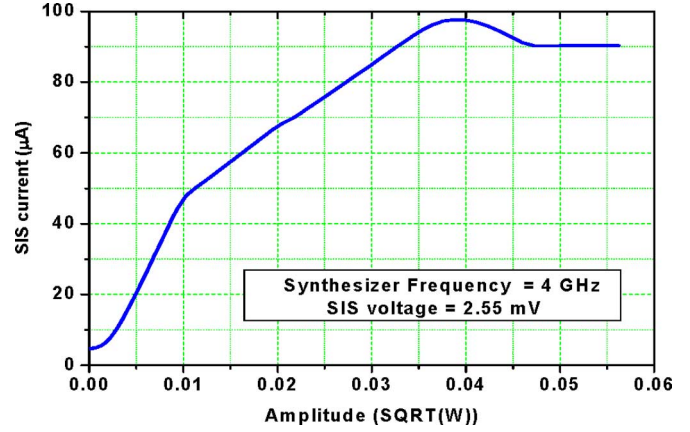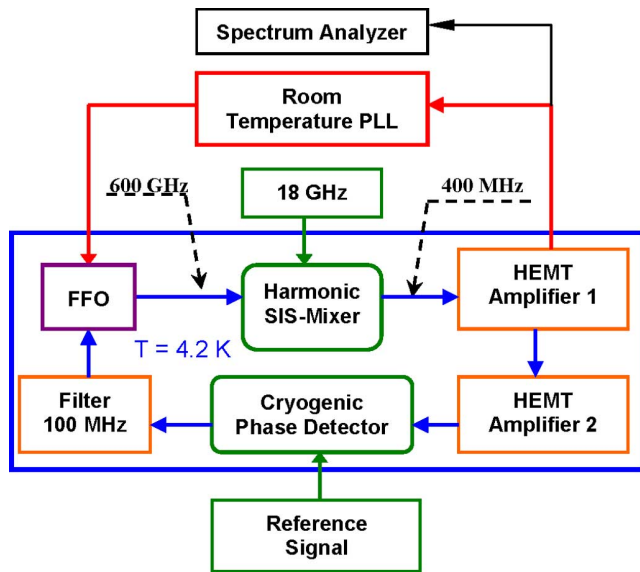
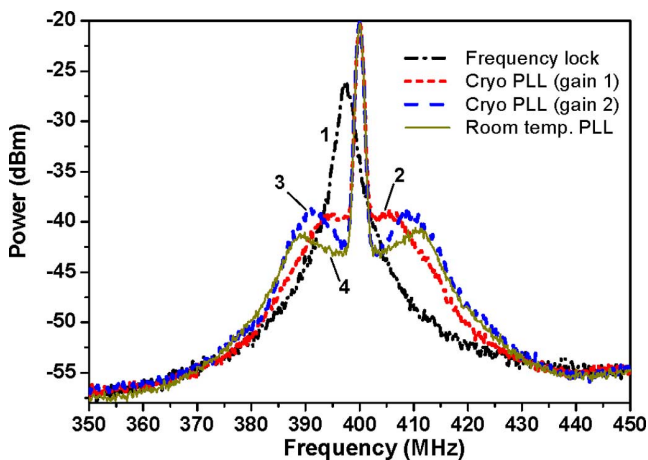Fig. 7. Block diagram of the experimental setup for CPD test.

Fig. 8. Down-converted spectra of the FFO operating at 600 GHz: curve "1"—frequency locked, "2", "3"—phase locked by CPD; "4"—phase locked by regular room temperature PLL.

common 10 MHz reference source. DC connections to the CPD are not shown in Fig. 7. The CPD can not provide a sufficient gain at low frequency to compensate slow drifts of the FFO; room temperature frequency lock system was used in parallel with the CPD to provide frequency stabilization of the FFO.

Obviously this first realization of the cryogenic PLL is far from the optimal; nevertheless it is possible to realize the FFO phase locking by the CPD. The first results are presented in Fig. 8 (curves 2 and 3 are measured at a slightly different gain of the HEMT-2). The linewidth of the frequency locked FFO

is 2.6 MHz (Fig. 8 curve 1). The obtained value of the SR (about 80% both for curves 2 and 3) is slightly lower than the value measured with the room temperature PLL system ($\mathrm{SR} = 83.5\%$, see curve 4). This is not surprising since the length of the CPD loop due to non-optimal realization is 1.6 m, which is close to the regular PLL. The estimation of the loop bandwidth [5] gives the value of about 5 MHz that is in the order-of-magnitude agreement with a experimental results. The phase noise of the FFO locked by CPD is -75 dBc/Hz at 100 kHz (that corresponds to results of regular PLL) while at 1 kHz offset the phase noise is considerably higher (-59 and -67 dBc/Hz respectively). Such deterioration of the performance at lower offset is because of absence of a amplifier and a specially design loop filter between the CPD and the FFO. A new system for the CPD test with improved performance is under design; preliminary results demonstrated that the CPD is very promising for a fully superconducting receiver.

IV. CONCLUSION

The first implementation of the Cryogenic Phase Detector seems very encouraging. Phase locking of an FFO by the CPD with the spectral ratio as high as 80% has been demonstrated in the preliminary experiments. A practical application of the CPD looks especially promising for the development of SIR arrays. Furthermore, the CPD may be used together with already developed SQUID pre-amplifier [6] and Flux-Flow amplifier [7] to realize optimal gain in the PL loop. Such combination would be a great step forward in development of the fully superconducting integrated array receiver.

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