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Optimization of superconducting microstrip interconnects for rapid single-flux-quantum circuits

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Abstract

In this paper, issues related to the optimization of superconducting passive interconnects are discussed. Results of the microwave optimization of bends, via connections and crossings of superconducting microstrip lines (SMSLs) are reported. The optimum design of the SMSL cross gives more than 95% of transmission and can be well used in a two-bus cross design with up to 14 signal wires. The results have been confirmed by time-domain simulations and measurements.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Availability of lossless passive interconnects is one of the major advantages of the rapid single-flux-quantum (RSFQ) superconducting digital technology [1]. Superconducting microstrip lines (SMSLs) allow long distance transmission of data pulses at the speed of light and with very high bandwidth (up to 750 GHz for Nb over SiO_2 at 4.2 K). The use of SMSLs for short range interconnects between circuit blocks and even between logic gates [2] benefits simplified circuit topology, reduced jitter and total bias supply current.

However, there are several problems that make use of SMSLs difficult in practical designs. First of all, accurate optimization of SMSL drivers and receivers is needed in order for reliable wider transmission of SFQ pulse energy through passive lines, between active superconducting devices [3, 4]. The second problem is a correct design of SMSL structures like bends, via connections between two different metallic layers, and crosses. These structures introduce impedance discontinuity and coupling that can substantially reduce the transmitted pulse energy and cause circuit malfunctioning [5]. Also, it is important to consider the minimum possible length of the short SMSL interconnects and correspondingly the maximum allowable length of the RSFQ cell inductances.

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The design of the different SMSL topologies should satisfy conflicting criteria: minimum occupied area, minimum reflection and minimum coupling. Screening of two crossing SMSL signal layers (figure 1(a)) is the most straightforward solution for coupling reduction [2]. However, this approach leads to a considerable increase in occupied area. For example, in the 2×2 RSFQ parallel multiplier described in [6], SMSL connections had been implemented with a screening layer and interconnects occupied more than 80% of the area. On other hand, direct SMSL crossing (figure 1(b)) leads to large capacitive coupling [7]. It should be noted that an advanced, submicron process of the future will use much narrower SMSLs.

This paper presents the results of 3D microwave optimization of SMSL bends, via connections and unscreened crosses. This paper has been organized as follows. Section 2 presents the models of a superconductor for microwave simulations. Section 3 describes the microwave optimization techniques and simulation results of the scattering matrixes (S parameters) for the optimized design in comparison with previous unoptimized designs. Section 4 gives the results of the time domain simulation of SFQ pulse propagation through the SMSL structures. In section 5, the critical dimensions of the lumped inductance in respect to the signal bandwidth are discussed. In section 6 the simulation results are compared with low- and high-frequency measurements and section 7 summarizes the paper.

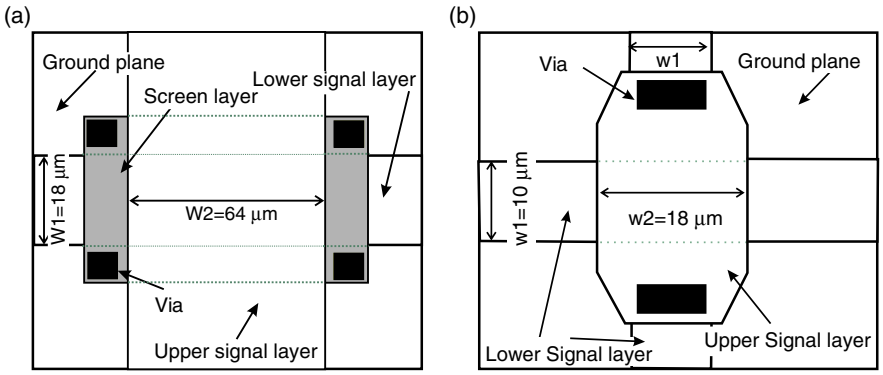

Figure 1. SMSL cross topologies: screened SMSL cross (a) and direct (unoptimized) SMSL cross (b).

Table 1. Superconducting microstrip's properties.

Model	$Z_0\Omega$	β	ε_{eff}	$L_{\text{sq}}pH$	$C_{\text{sh}}fF$
Theoretical values	4.7	18 339	8.51	0.46	0.207
Perfect conductor model for HFSS	3.82	15 949	6.43	0.3232	0.215
Perfect conductor model for Sonnet	3.97	16 087	6.5463	0.3388	0.215
Complex conductivity model for Sonnet	4.6	18 766	8.91	0.458	0.217
Built-in superconductor model of Sonnet	4.6	18 766	8.91	0.458	0.216
Resistive surface model for HFSS	4.47	18 110	8.9586	0.43	0.215

2. Superconductor model for the SMSL

Two commercially available 3D electromagnetic simulators, HFSS [8] and Sonnet [9] were considered for optimization of the SMSL structures. Due to the absence of an inherent accurate model for superconductors in either of the two simulators, superconducting microstrips were modelled as a resistive surface conductor (HFSS) and a conductor with complex conductivity (Sonnet). The calculated results of impedance (Z_0), wave propagation constant (β) and effective dielectric constant (ε_{eff}) were compared with theoretical values and with results for a perfect conductor model.

Following [10], the resistive surface conductor model of superconductor can be expressed in the following equations for the real part (R_{sur}) and imaginary part (X_{sur}) of the surface impedance:

$$R_{\text{sur}} = \frac{2\pi\omega^2\lambda_{\text{L}}}{c^2}\frac{n_{\text{n}}}{n_{\text{s}}}\tau, \qquad X_{\text{sur}} = \frac{4\pi\lambda_{\text{L}}\omega}{c^2}, \tag{1}$$

where $\tau = \frac{l}{V_{\text{F}}}$, l is the mean free path of an electron and V_{F} is the velocity of an electron, $\frac{n_{\text{n}}}{n_{\text{s}}} = (\frac{T}{T_{\text{c}}})^4$, n_{n} is the normal electron density, n_{s} is the Cooper pair density, T is the operating temperature in kelvin, T_{c} is the critical temperature, and λ_{L} is the London penetration depth.

The expressions for the real and imaginary parts (σ_1 and σ_2 respectively) of the complex conductivity model are as follows:

$$\sigma_1 = \frac{n_{\text{n}}}{n_{\text{s}}}\frac{\tau}{\Lambda}\left[\frac{1}{1+(\omega\tau)^2}\right], \qquad \sigma_2 = \frac{1}{\Lambda\omega}\left[1+\frac{n_{\text{n}}}{n_{\text{s}}}\frac{(\omega\tau)^2}{1+(\omega\tau)^2}\right], \qquad \Lambda = 4\pi\frac{\lambda_{\text{L}}^2}{c^2}. \tag{2}$$

For clean Nb at 4.2 K with $\lambda_{\text{L}} = 54$ nm and $\tau = 1 \times 10^{-12}$ s, the models give $R_{\text{sur}} = 1.2979 \times 10^{-4}$ Ω, $X_{\text{sur}} = 0.0204$ Ω, and $\sigma_1 = 1.0642 \times 10^7$, $\sigma_2 = 9.1286 \times 10^8$.

Table 1 summarizes the simulation results for SMSL designed for the NGST 8 kA cm^{-2} Nb fabrication process [11]. The signal wire is a 150 nm thick ($\lambda_{\text{L}} = 54$ nm) lower wiring layer separated from the ground plane by two insulation layers: 144 nm thick N_2O_5 and 159 nm thick SiO_2. The width of the SMSL is equal to 10 μm, that corresponds to the 4.7 Ω impedance. The parameters have been estimated at 300 GHz frequency, corresponding to the typical SFQ pulse bandwidth. The SFQ pulse bandwidth is determined by the width of the Gaussian fit of the SFQ pulse spectra at the SMSL driver and receiver.

Table 1 shows that in the case of HFSS's resistive surface model and Sonnet's complex conductivity model results are in a good agreement with theoretical estimations, when in the case of a perfect conductor there are considerable deviations. Since HFSS is more accurate than Sonnet for simulation of 3D complex structures, later in this paper all given results have been obtained with the HFSS resistive surface model.

3. Microwave optimization of SMSL structures

This section presents simulated S parameters and optimized layouts of the following SMSL structures: bends, via connections and crosses. These structures were simulated and optimized for the 8 kA cm^{-2} NGST fabrication process and the 1 and 4.5 kA cm^{-2} Hypres [12] fabrication process. SMSL parameters for these three processes are summarized in table 2.

3.1. SMSL bend

The big corner inductance of a right-angle SMSL bend introduces considerable impedance discontinuity and a well

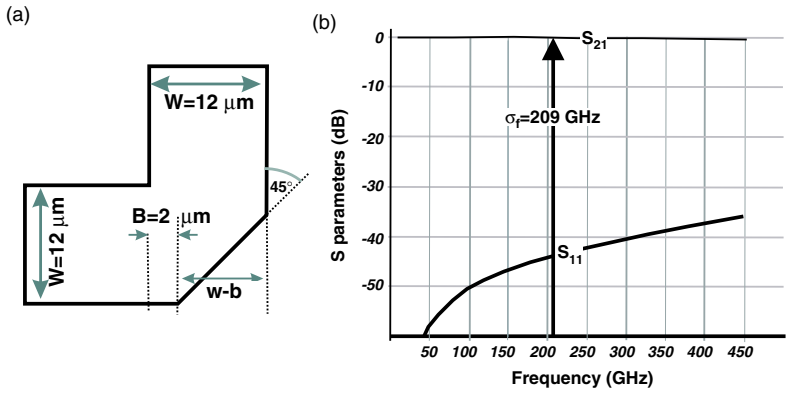

Figure 2. Topology of SMSL right-angle bend optimized for the Hypres 4.5 kA cm^{-2} process (a) and corresponding S parameters (b).

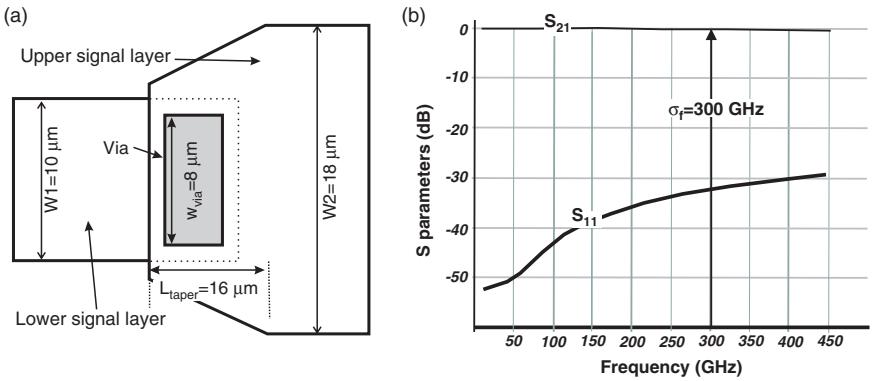

Figure 3. Topology of SMSL via connection optimized for the NGST 8 kA cm^{-2} process (a) and corresponding S parameters (b).

Table 2. Electrical parameters of SMSL of the lower wiring layer for different fabrication processes.

J_c	1 kA cm^{-2} Hypres	4.5 kA cm^{-2} Hypres	8 kA cm^{-2} NGST
w (μm)	18	12	10
L_{sq} (pH)	0.41	0.455	0.46
C_{sh} (fF)	0.277	0.277	0.209
Z_0 (Ω)	2.13	3.342	4.7
σ_f (GHz)	156	209	300
λ_ω (μm)	603	450	331
v (m s^{-1})	0.941×10^8	0.941×10^8	0.993×10^8

known method to reduce this effect is to cut a mitre [13]. Figure 2(a) presents an SMSL right-angle bend optimized for Hypres 4.5 kA cm^{-2}, where a 45° mitre with dimension $b \approx w/6$ gives quite good matching with maximum -44 dB reflection losses at signal frequency (figure 2(b)).

3.2. SMSL via connection

Impedance discontinuity also occurs at connections between two SMSLs with signal wires designed in different layers. An example of such a connection designed for the NGST 8 kA cm^{-2} fabrication process is shown in figure 3(a). Signal wires have been designed in the first and the second wiring layers with corresponding widths given by $w1 = 10$ μm and $w2 = 18$ μm, providing equal impedance of both wires. In order to reduce reflection losses, the connection between two signal wires has been designed with tapered topology and possible widest via hole [14]. Figure 3(b) presents the return losses and transmission scattering matrix for the optimized via connection with -32 dB reflection loss at signal frequency.

3.3. SMSL cross

Crossing two signal wires without additional screening results in a quite noticeable coupling and also introduces impedance discontinuity. The example of such a cross with unoptimized topology is shown in figure 1(b). The particular design has -18 dB of coupling and -9 dB of losses (see figure 4(a)). This design has been used in an RSFQ parallel multiplier [15]. The strong coupling and big return losses were unacceptable for the circuit. As is shown in the Smith chart of figure 4(b)), the coupling is mainly capacitive due to the big overlapping area between signal wires.

In order to reduce coupling, both SMSL signal wires have to be narrowed at the cross and tapered topology can be used to reduce the impedance discontinuity. Figure 5(a) shows the topology of the cross optimized for the Hypres 4.5 kA cm^{-2} process: the width of the lower signal layer is equal to $w1 = 12$ μm and that of the upper signal layer is equal to $w2 = 25$ μm; the lengths of tapers are $l1 = 8$ μm and $l2 = 16$ μm correspondingly. Figure 5(b) shows the reflection and coupling for this design. This optimized cross

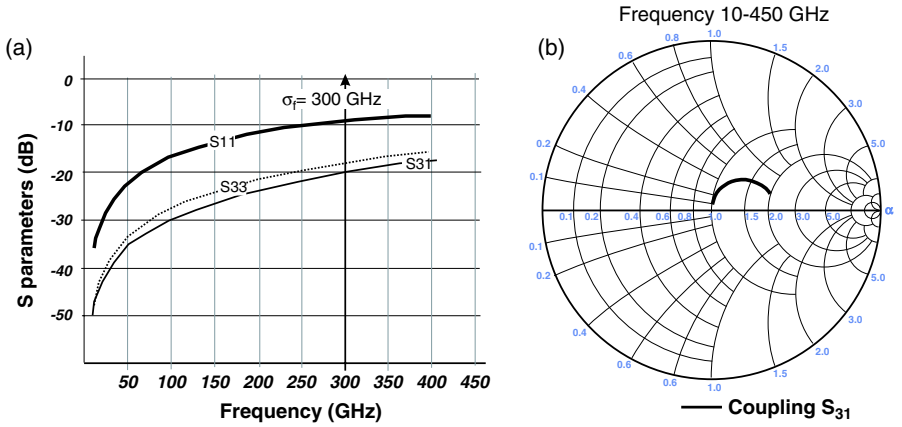

Figure 4. S parameters of unoptimized SMSL cross for the NGST 8 kA cm^{-2} process (a) and the corresponding Smith chart.

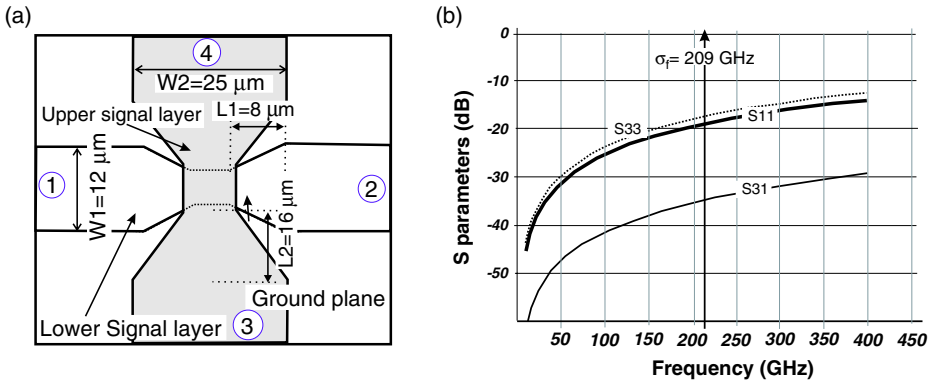

Figure 5. SMSL cross optimized for the Hypres 4.5 kA cm^{-2} process and (a) corresponding S parameters.

has −36 dB coupling and less than −19 dB of reflection losses at signal frequency.

Similar data for the cross optimized for the Hypres 1 kA cm^{-2} process is presented in figure 6. The optimized parameters of the cross are the following: the width of SMSL in the lower signal layer is equal to $w1 = 18$ μm and that in the upper signal layer is equal to $w2 = 32$ μm; the lengths of tapers are $l1 = 6$ μm and $l2 = 5$ μm. This optimized cross has −26 dB of coupling and less than −50 dB of reflection losses at signal frequency. For comparison, the figure shows also S parameters for the straightforward screened cross design shown in figure 1(a). The screened design has negligible coupling, but quite noticeable reflection losses and big area. Comparison between the screened and optimized unscreened designs favours the latter.

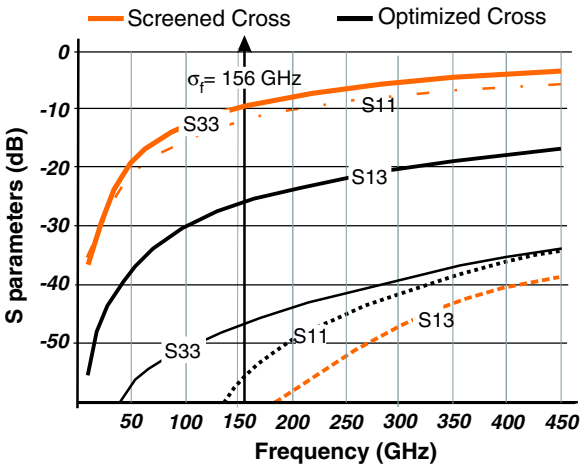

Figure 6. S parameter of the screened and the optimized cross for the Hypres 1 kA cm^{-2} process.

4. Time domain simulation of SFQ pulse propagation

In order to verify the SFQ pulse propagation through the SMSL cross, time domain simulations have been done using the PSCAN software package [16]. The simulated circuit consists of two SMSLs connected to drivers and receivers and having intersection with each other through the inserted SMSL cross. Parameters of drivers, receivers and the SMSL have been optimized for a 1 mm long SMSL following the procedure described in [6]. The distributed L–C model of the SMSL has been used for the simulation, with the length of each segment less than $\lambda/20$. During the simulation, two pulse trains have been sent to SMSLs. A pulse train with eight pulses and period of 25 ps (40 GHz) marginalized to the fastest case has been sent to the reference SMSL and another pulse train consisting of 15 pulses and variable period has been sent to the SMSL under test.

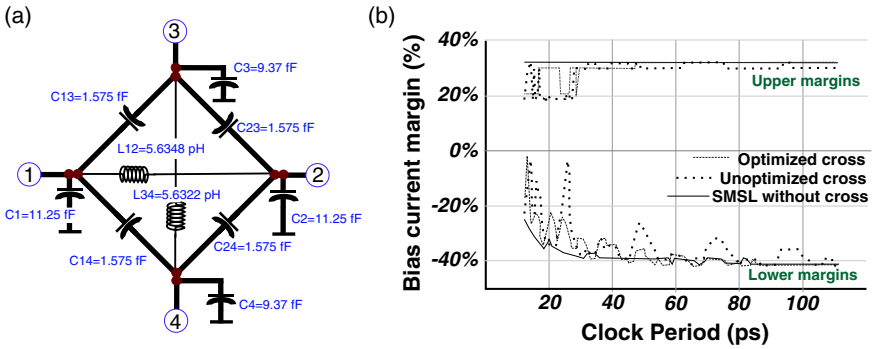

Figure 7. Extracted equivalent circuit of the SMSL cross optimized for the NGST 8 kA cm^{-2} process (a) and corresponding global bias margins for SFQ pulse propagation (b).

An automatic procedure has been applied to extract the equivalent circuits of the SMSL crosses. The extraction procedure takes as an input scattering matrix parameters for the bandwidth corresponding to a certain fabrication process. Equations of the parameters for the equivalent circuit have been evaluated on the basis of π-network topology by solving the equations of the scattering matrix for given input [14]. An example of the equivalent circuit of the cross optimized for NGST 8 kA cm^{-2} is shown in figure 7(a).

Figure 7(b) shows the global bias current margins for the simulated circuits with optimized and unoptimized crosses in comparison to margins for single SMSL. The curves typically have peaks corresponding to simultaneous arrival of the SFQ pulses from both SMSL lines to the cross. The highest peak corresponds to the same clock period in both SMSLs. The optimized design drastically increases margins from almost 5% up to 22% at the highest peak. In the regions where there is no colliding of the pulses at the cross, the margins reduced by at most 8% in comparison to the ordinary SMSL. This margin reduction is due to the reflection losses and corresponding geometrical resonance. This is the general result and valid for all the fabrication processes.

By interleaving the pulses at the cross and adjusting the SMSL length and clock period, total insertion losses of the SMSL cross can be less than 1% in terms of operational margins. Keeping the usual 30% margin criteria on global bias current, SMSL interconnects can have about 14 optimized crosses without severe degradation of circuit operation.

5. Dimension of lumped inductance

The lumped inductance's capacitance to the ground has significant effect on the timing parameters of the circuits. In order to study this effect, an RSFQ D flip-flop circuit with distributed model for quantized inductances has been simulated. The parameters were optimized for the Hypres 4.5 kA cm^{-2} process with the PSCAN software package. During the simulation, the length of the inductance has been varied. The D flip-flop has been optimized for stable and faster operation and a certain timing parameter following the developed procedure for RSFQ gates [17].

Figure 8 shows the global bias current upper margin versus the inductance's length normalized on wavelength (λ) of a given frequency for different numbers of distributed L–C units. The margin is more than 30% and steady when the length of the inductance is less than $\lambda/4$. The curves have small peaks at the position where the length of inductor is equal to half of the wavelength due to the presence of a standing wave at that length. The curves show that an increase in number of L–C units improves the accuracy of the margin calculation.

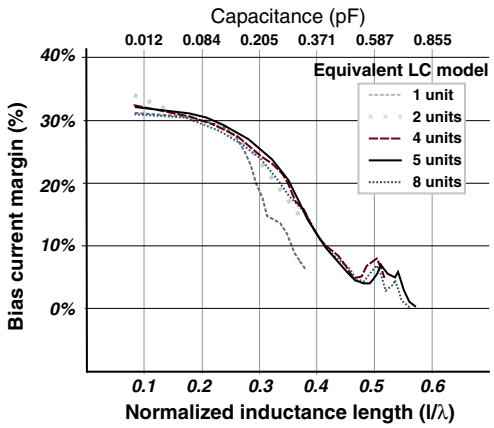

Figure 8. Bias current margin for different lengths of the inductance as normalized on wavelength (l/λ).

Figure 8 indicates that an increase in the inductance length more than $\lambda/4$ leads to a sharp decrease of operating margins. The maximum length of inductance is 112 μm for the Hypres 4.5 kA cm^{-2} and 83 μm for the NGST 8 kA cm^{-2} process. The maximum length of inductance scales down with an increase of J_c like

$$L_{\text{feature}} \propto \frac{1}{\sqrt{J_c}}. \tag{3}$$

Therefore in order to get the desired operational margin, the feature size needs to be decreased with increase in J_c.

6. Experimental results

To verify the developed methods for SMSL optimization, test structures for low frequency and high frequency tests have been designed and fabricated with the NGST 8 kA cm^{-2} and Hypres 4.5 kA cm^{-2} fabrication processes. All experiments have been done using an automated data acquisition system, 'Octopux' [18]. All the test structures have been simulated with the procedure similar to the experiment.

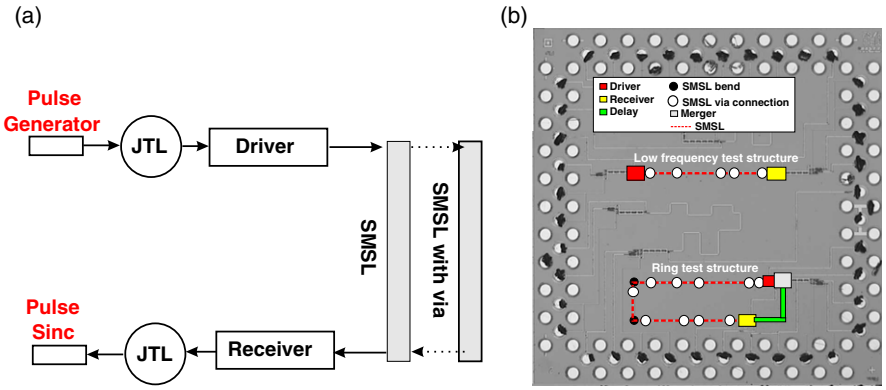

Figure 9. Low frequency test circuit (a) and microphotograph of the test structures for SMSL interconnects for the NGST 8 kA cm^{-2} process (b).

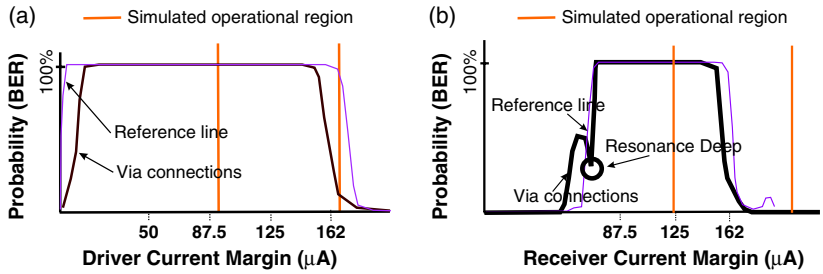

Figure 10. Low frequency via connection measurement results: driver (a) and receiver (b) bias current.

Two test structures have been designed for low frequency tests (figure 9(a)): a single SMSL connected to the driver and receiver and a similar SMSL with inserted 10 via connections. Both circuits have been fabricated with the NGST 8 kA cm^{-2} process. The goal of the experiments was to compare margins of bias current of the driver and the receiver for both structures. A microphotograph of the fabricated chip is shown in figure 9(b). The layout for via connection is same as shown in figure 3(a). The low frequency test pattern of 1000 pulses has been applied to the driver to perform bit error rate (BER) measurements.

Figure 10 shows the probability curves for different driver and receiver bias currents. At each measurement either driver or receiver bias current has been kept at its nominal value. The thin lines give the reference margin of the simple SMSL. The thick lines present the results for the SMSL with via connection. The vertical lines represent boundaries of the simulated working region.

Experimental data of margins, that determined the 100% probability of pulse transmission, was wide, up to ±62.5% for the driver and ±42.5% for the receiver, and were the same for the single SMSL and the SMSL with via connections. The operational margins were shifted in comparison to the simulation results, that can be addressed to accumulate spread in all fabrication parameters. Taking this shift into account, the simulation and measured data are in good agreement.

Following the approach proposed in [19], two test structures have been designed for high frequency tests (figure 12(a)): an SMSL with 20 inserted via connections connected to the driver and receiver in a ring and a similar ring with an SMSL with 16 inserted right-angle bends. Circuits have been fabricated with the Hypres 4.5 kA cm^{-2} and NGST 8 kA cm^{-2} processes. The goal of the experiments was to measure margins of the driver bias current for different frequencies. A microphotograph of the chip fabricated with Hypres 4.5 kA cm^{-2} is shown in figure 11(a). The layouts for bend and via connections are the same as shown in figures 2(a) and 3(a). During the experiment, a single pulse has been injected into the ring. In each ring there was indeed a JTL delay with 20 junctions. The speed of the pulse rotation has been tuned by varying the bias current of delay line. The circuits have been designed for 7–14 GHz; the choice of frequency is a compromise between frequency and ability to tune the frequency.

Figure 12(b) presents the measured driver bias current margins. At each measurement the receiver bias current has been kept at its nominal value. The thick black lines are the margins for ring test structures for via connections. The thin black lines are the experimental results for a test structure with bends. The dotted lines are the simulated results.

Measured margins were ±30% or more for driver bias current except some peaks for a certain frequency range. There are peaks in the margin for via connections at 10–11 GHz, which is in good agreement with simulated results. This frequency range corresponds to four times the pulse propagation time through the SMSL of the ring. The measured margins for test circuits with bends are more than 30% except for some peaks at 3 and 6 GHz due to structural resonances.

A separate high frequency test circuit has been designed to test cross coupling between SMSLs (figure 13(a)): two rings crossing each other with a simple SMSL. The circuit has been fabricated with the Hypres 4.5 kA cm^{-2} process (figure 11(b)).

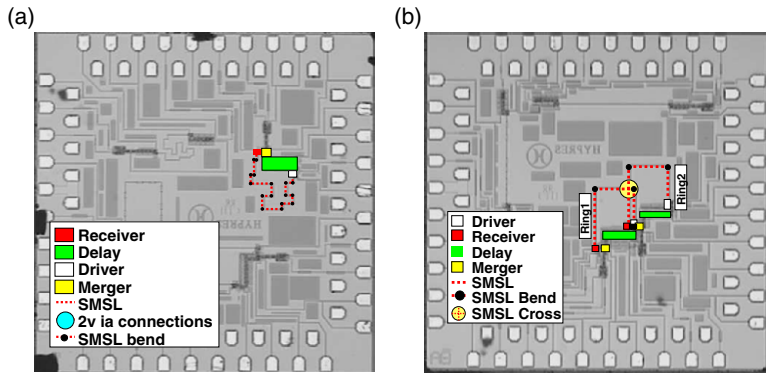

Figure 11. Microphotographs of the test structures for SMSL interconnects: ring (a) and double-ring (b) test structures.

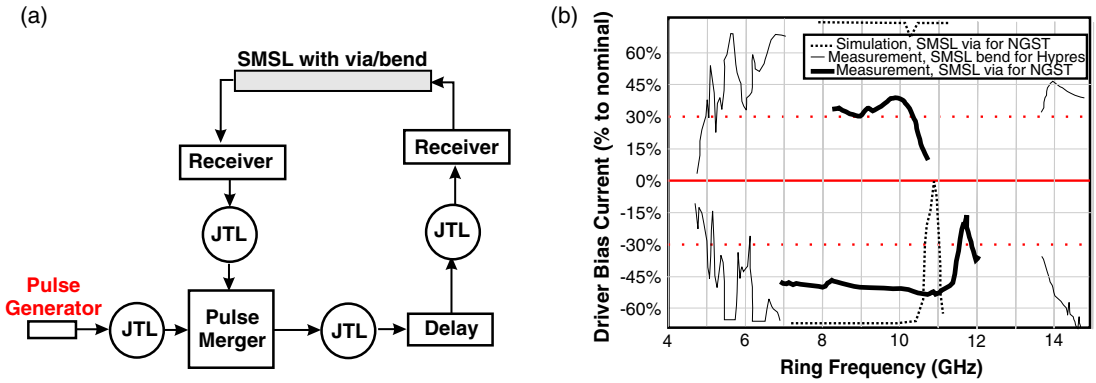

Figure 12. Ring test circuits (a) and measurement result for driver bias current (b).

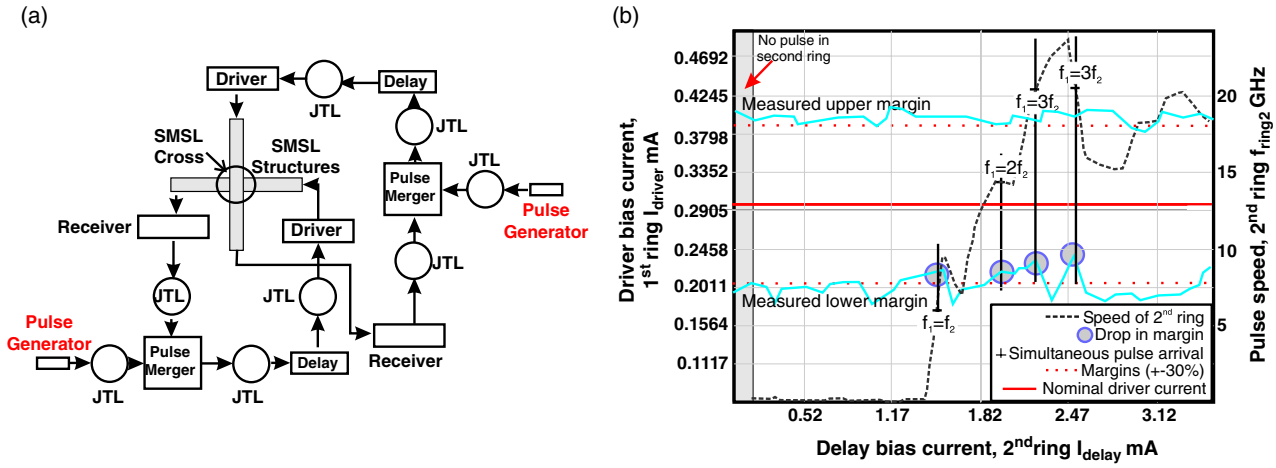

Figure 13. Double ring test circuits (a) and measurement result for driver bias current (b).

Layouts for the optimized SMSL cross are the same as shown in figure 5(a). During the experiment, a single pulse has been injected into both rings and the delay of the first ring has been varied to vary the pulse rotation frequency.

Figure 13(b) presents the measured driver bias current versus the delay bias current of other ring. At each measurement the receiver and delay bias current of the corresponding ring have been kept at their nominal values. The thick lines are the margins. The dotted line is the measured pulse rotation speed of the other ring. The black vertical lines are the point when all pulses of the first ring coincide with pulses of the second ring.

Experimental data for the margins are almost constant to $\pm 30\%$ and are independent of whether there are pulses or not in the other ring. This indicates nearly zero coupling between SMSLs. The lower bias margin has peaks when all pulses of the ring coincide with pulses of the other ring. This experiment justifies the simulation results of figure 7(b) that the lower bias

current margin will drop when all pulses of one SMSL will coincide with pulses of the other SMSL as the cross.

7. Conclusion

This paper presents techniques for optimization of the superconducting microstrip line (SMSL) used as passive interconnects in large scale integrated (LSI) RSFQ circuits. The components that have been considered are SMSL bends, via connections and crosses. The goal of optimization was to reach maximum transmission of signal at the frequency bandwidth of SFQ pulses and minimization of the occupied area. The optimization has been done for three different processes: the NGST 8 kA cm^{-2} and the Hypres 4.5 and 1 kA cm^{-2} fabrication process. All the optimized structures have good transmission properties: -8×10^{-5} dB for the bend, -1.2×10^{-3} dB for the via connection and -4.48×10^{-2} dB for the cross. In comparison with previously published results, this gives a large improvement in transmission and allows us to reduce the area for interconnects.

The results have been confirmed by time domain simulation and low and high frequency measurements. The experimental data give $\pm 30\%$ margins for the SMSL driver and receiver. There was no considerable coupling detected in the high frequency test. In conclusion, the suggested method for SMSL optimization can be successfully used for any fabrication process. The optimum design allows us to apply SMSL for LSI RSFQ circuits with up to 16 crossing lines.

Acknowledgments

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