Submillimeter Superconducting Integrated Receivers: fabrication and yield

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***Abstract*—fabrication procedure and yield analysis of the superconducting integrated receivers is reported. These chip receivers, apart from the quasi-optical SIS mixers, contain internal local oscillators and associated rf and dc interface. Due to both complexity and design requirements of the integrated circuit, certain restrictions are applied to the standard Nb/Al/Al_xO_y/Nb SNEAP process. To obtain accurate area for micron-size SIS junctions and thickness for multi-layer SiO_2 insulation, a few solutions and modifications were developed. The possibility of transfer this fabrication process worldwide has been proven experimentally.**

***Index Terms*—Josephson effect, lift-off process, Nb technology, RIE process, SIS junction, SIS mixer, SIS receiver, SNEAP process, submillimeter receiver, superconducting tunnel junction.**

I. Introduction

SUPERCONDUCTING Integrated Receiver (SIR) is a unique integrated circuit comprising two active devices: ultra-low-noise SIS mixer and Josephson local oscillator (LO) built on the base of flux-flow oscillator (FFO). A number of receiver chips have been designed, fabricated and tested since 1992 in IREE (Moscow, Russia) and SRON/FDL (Groningen, the Netherlands), covering the frequency range of 100 – 700 GHz [1] - [4]. The devices are useful for a wide range of applications, where extreme compactness and low power consumption are of great importance, e. g. for the multi-channel detection from board of air- or space-born observatory or the laboratory study of emission from variety of coolable devices [5]. The new ambitious radio astronomy multi-dish projects (e.g. ALMA [6]) would gain considerably by using single-chip SIRs due to their lower price and better serviceability as compared to conventional approaches. In this paper we report briefly on fabrication procedure and main test results of the submillimeter quasi-optical SIRs for frequency range of 400 - 700 GHz.

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To set the practical requirements to the fabrication process, the extensive numerical simulation of the whole integrated circuit have been performed [7]. There are a few design problems, which are worth to mention here. The LO power has to be coupled from the low-impedance FFO to the SIS mixer via a relatively long microstrip transmission line, which has to provide the exact proportion between coupled and reflected powers. To realize this, the rf loss of all materials have to be either negligible or well defined.

A number of key elements of the circuit have to be fabricated quite accurately. The area of a micron-size mixing SIS junction defines not only exact tuning frequency, but also pump level and loss of the signal towards LO. The narrowest strip of the circuit is the LO power injection chain of 1.5 μm wide. Its accuracy has to be of order of 15% or about 0.2 μm.

According to present design, accurate alignment of all layers is of great importance. To provide the SIS mixer with strong enough magnetic field, the narrow, 3 μm wide, control line is laid on top of the junction, that means misalignment less than 1 μm. The challenge of the project was to fabricate the whole circuit using the routine procedure developed for SIS mixers, that is based on a standard optical photo lithography.

II. Fabrication Procedure

A general view of the integrated circuit is presented in Fig. 1. According to the rf requirements the substrate must be a part of the optical system, i. e. must be from the same (or similar) material as the microwave lens. This brings some difference in fabrication procedure for the quartz [1], [2] and for the silicon optics [3]. The main steps of the fabrication process are presented schematically in Fig. 2, that is, basically, modified SNEAP procedure [8], [9]. The layers and their deposition parameters are listed in Table I.

To achieve both visual control of the reactive ion etching (RIE) during the junction definition and good patterning of AZ5214E image reversal photo-resist, the monitor layer from Nb is deposited on the optically transparent substrate (mono-crystalline quartz 15 by 24 millimeters) using dc magnetron. For the case of 2-inch silicon wafer, the monitor layer is not usually used, but a protection layer of Al_2O_3 is deposited by rf magnetron. This layer is needed to eliminate the over-etching of the silicon substrate during RIE process. The base electrode of the whole structure is defined by the lift-off (see (1) in Fig. 2). The Nb–Al/Al_xO_y–Nb trilayer is formed *in situ*; both metals, Nb and Al, are sputtered by dc magnetron is formed on the surface of aluminum film with its native

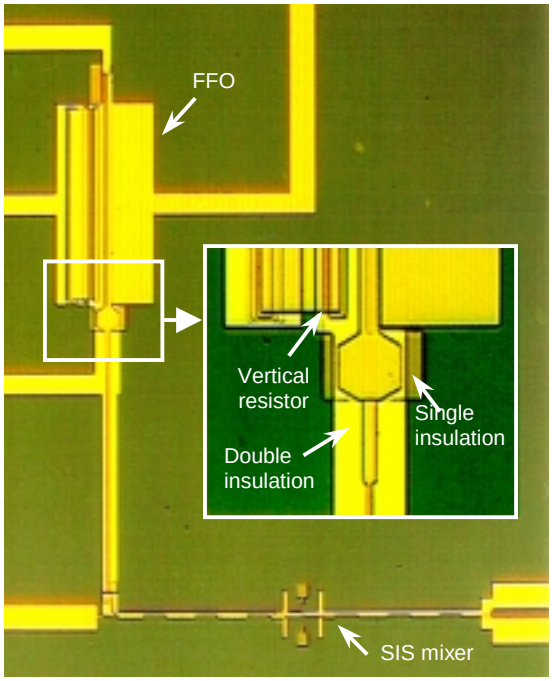

Fig. 1 General view of central part of chip receiver. The inset presents magnified view of the FFO impedance transformer where two different layers of insulation are used.

oxide (Al_xO_y) at room temperature. The Leybold-560 and Nordiko-2000 sputtering machines were used in IREE and SRON/FDL accordingly.

To define a micron-size window SIS junction, two methods were used. The first method, which can be named as the traditional one, includes a square window in SiO_2 insulation. The second method is so-called cross-bar (or cross-line) definition [10], [11]. It is important to remind here that, for reasons of rf design, two layers of insulation are used in the integrated circuit. In both cases two overlapping windows are formed using SNEAP process with SPR2-1.3FX positive photo - resist; (2) - (5) from Fig. 2. The difference is that for a square junction the first window (1 μm by 1 μm) of the *two coaxial windows* is defining the junction area, while for a cross-bar junction the resulting window is the *overlapping area of two perpendicular slots* of size 1 μm by 6 μm each. The photograph of the junctions formed by these two methods is presented in Fig. 3. The monitor layer is very helpful for the traditional single step definition process; it is used to

TABLE I
LIST OF LAYERS

Material	Destination	t (nm)	Parameters of deposition
Al_2O_3	buffer layer	100	Ar, 20 mTorr, 0.75 nm/s
Nb	monitor layer-1	100	Ar, 8 mTorr, 1.5 nm/s
Nb	bottom electrode	100/200	Ar, 8 mTorr, 1.5 nm/s
Al/Al_xO_y	barrier	7/1	Ar, 8 mTorr, 0.36 nm/s, O_2, 10 mTorr, 20 min
Nb	top electrode	100	Ar, 8 mTorr, 1.5 nm/s
Al_2O_3/Nb_2O_5	anode insulation	7-11	7.5-10 Volts
SiO_2	insulation-1	150	Ar, 20 mTorr, 0.24 nm/s
Al_2O_3/Nb_2O_5	anode insulation	7-11	7.5-10 Volt
SiO_2	insulation-2	100	Ar, 20 mTorr, 0.24 nm/s
Al	resistor	200	Ar, 8 mTorr, 0.36 nm/s
Nb	monitor layer-2	20	Ar, 8 mTorr, 1.5 nm/s
Nb	wiring	600	Ar, 8 mTorr, 1.5 nm/s
Al	protection layer	50	Ar, 8 mTorr, 0.36 nm/s
Al/Au	contact pads	10/95	Ar, 8 mTorr, 3.0 nm/s

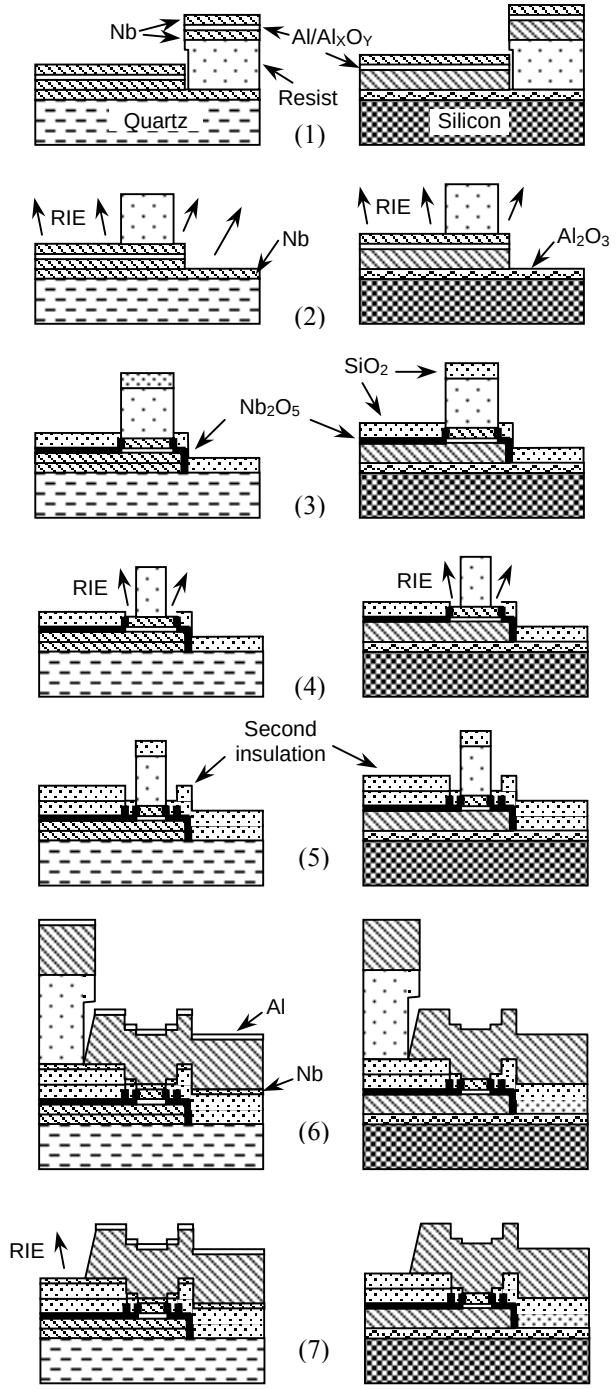

Fig. 2 Fabrication steps for Superconducting Integrated Receiver for quarts optics (left column) and for silicon optics (right column): (1) definition of base electrode and trilayer deposition, (2) first window definition, (3) RIE, anodization and *first* insulation deposition, (4) second window definition and RIE, (5) anodization and *second* insulation deposition, (6) wiring electrode definition; two additional layers from Nb and Al are used in case of quartz substrate, (7) final cross-section; the Au layer process not included.

visually estimate the end of the RIE [13]. This information is used for monitoring of the second RIE of the cross-bar junction. The typical RIE parameters were: 250 mbar of mixture CF_4+3%O_2 at 35 W. The insulation layers were sputtered in Z400 by rf magnetron.

The bias resistor for the FFO (see Fig. 1) is formed on the place of a large SIS junction. To remove the top electrode of the trilayer, this large "junction" is etched by RIE, which stops at the Al layer. The barrier aluminum of the trilayer is removed by wet etching. The normal metal (i. e. resistive layer) is deposited in place of the tunnel barrier using lift-off process. Finally, the resistor is connected by the wiring film, which is patterned using AZ5214E image reversal photo-resist.

To obtain good patterning of the wiring layer, the additional Nb film (20 nm) is deposited as shown in Fig. 2 (6) for the case of a transparent substrate. This layer prevents the photo-resist from reflected UV light and has to be etched after lift-off; thin Al film is used as an RIE mask for the wiring electrode, Fig. 2 (7). The examples of submicron alignment are presented in Fig. 3 and Fig. 4. The pads for spring contacts/bonding are gold-plated (see Table I).

III. Results and Discussion

The dc characteristics of the circuit were measured with data acquisition (DAQ) system IRTECON [3], [14]. This DAQ system was developed as a dedicated tool for test and control of the Superconducting Integrated Receiver. Fig. 5(a) presents typical IV-curve of the SIS mixer. The R_NA product

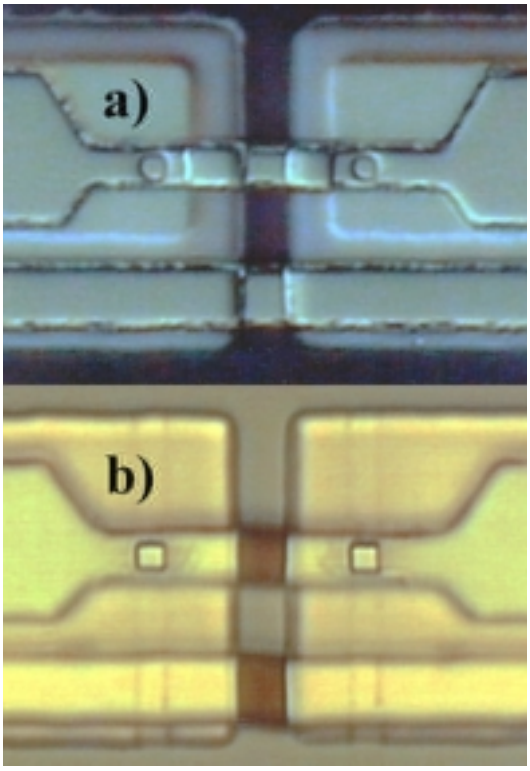

Fig. 3 Examples of definition of SIS junction for balanced mixer [3], [4]: single step windows (a) and cross-bar windows (b) The area of junctions is about 2 micrometers; alignment accuracy is better than 0.5 μm.

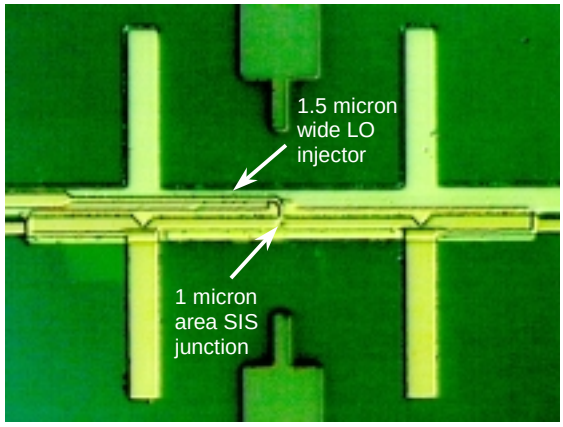

Fig. 4 Magnified view of quasi-optical double-dipole antenna mixer from Fig. 1. This is another example of precise alignment of a micron-size SIS junction within 3 μm wide control line.

of micron-size SIS junctions was in the range of 25-30 that corresponds to the current density of 7-8 kA/cm^2.

It is possible to see from Fig. 3, that cross-bar junctions (b) are shaped better, than ones of the single-step definition (a) (note rounding of the corners). Similar to [11], we have found that the second RIE for the cross-bar junctions has to be a few times longer. It can be explained by difficulty in etching through the micron-narrow slots in the first SiO_2 insulation. Sometimes, as the result of non-complete etching, the IV-curve of the SIS junction had smeared gap structure. To obtain proper thickness of the insulation, the second layer was made thicker being corrected to the etching rate of SiO_2, which was estimated as 0.1 nm/s.

The accuracy of the top wiring in the srtipline is important for both the frequency tuning of the SIS mixer and the proper coupling of LO power. The tuning strips of the SIS mixer plays also a role as a control line [2], [3], whose characteristic is shown in Fig. 5(b). It demonstrates a good Fraunhofer pattern up to the third minimum of the critical current. The magnetic field up to about 40 kA/m can be achieved with the current of 150 mA. It was found, that the edge profile of the control line, which is a 3 μm wide strip on top of the SIS junction (see Fig. 3 and Fig. 4), can influence the critical current of this strip. In a few batches, samples, which were good-looking with an optical microscope, had the critical current less than 20 mA. The problem has been identified by SEM inspection (see Fig. 6). As it is drawn in Fig. 2(6), there is a tendency of trapezoidal edge of the film patterned with an undercut profile of photo-resist. One can assume that the trapezoidal profile considerably facilitates the entrance of Abricosov vortexes in the film and consequently reduces its critical current. It have been found, that the problem can be solved either by processing the photoresist with less undercut profile or by use of positive resist, that, unfortunately, can not guaranty smooth edges of the lift-off film.

The quality of IV-curve of the flux-flow oscillator is usually the same as for the SIS mixer. The critical current of the FFO can be suppressed completely with magnetic field produced by the integrated control line implemented in the base electrode (see Fig. 1 and also [2]-[4]), that means a good

quality of the tunnel layer over a large area of 450 μm by 4 μm.

To characterize the yield of SIR devices, the final rf test data should be mentioned. For example, all 9 pixels of the

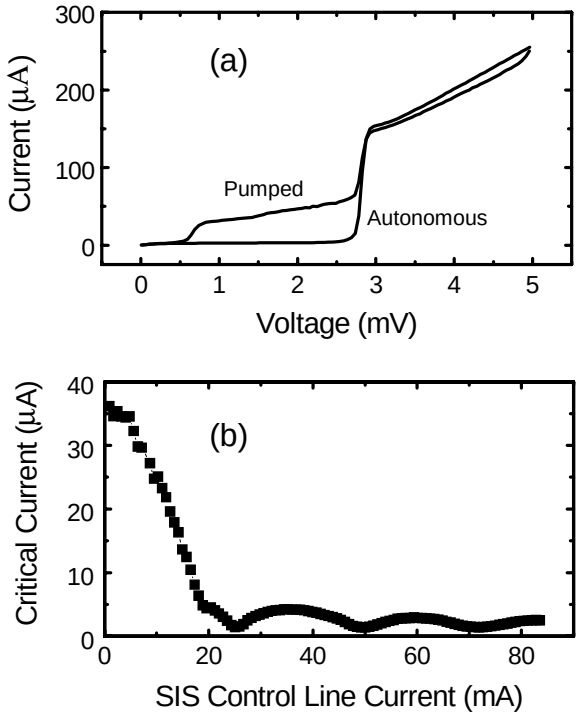

Fig. 5 Main characteristics of the SIS mixer: IV-curves, autonomous and pumped by FFO at 500 GHz (a) and control line characteristic (b).

500 GHz Imaging Array Receiver [3], [4] were selected from two batches. This selection of nearly identical devices was made from two groups of only 20 devices each. The yield of a good batch was up to 80% according to the dc pre-test and up to 25% after the rf selection.

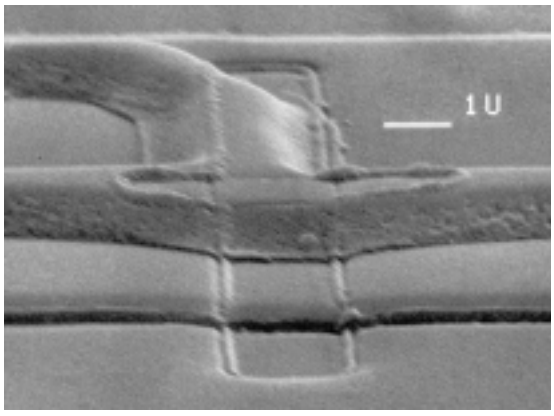

Fig. 6 SEM photograph of a cross-bar SIS junction, indicating trapezoidal profile of wiring, that can lead to up to one order degradation in critical current of the SIS mixer control line.

IV. Conclusion

A procedure of fabrication of Superconducting Integrated Receiver has been developed successfully using optical photo lithography and proven to be transferable from one lab to another. This development confirms the possibility of massive production of receiving chips containing FFOs, SIS mixers and rf coupling circuits from Nb operating at sub-terahertz frequencies.

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References

[1] V. P. Koshelets, A. V. Shchukin, S. V. Shitov, and L. V. Filippenko, "Superconducting millimeter wave oscillators and SIS mixers integrated on a chip", *IEEE Trans. on Appl. Supercond*., vol. 3, No. 1, pp. 2524-2527, 1993.

[2] V. P. Koshelets, S. V. Shitov, L. V. Filippenko, A. M. Baryshev, H. Golstein, T. de Graauw, W. Luinge, H. Schaeffer, H. van de Stadt, "First implementation of a superconducting integrated receiver at 450 GHz", *Appl. Phys. Lett*., vol. 68 (9), pp. 1273-1275, 1996.

[3] S. V. Shitov, V. P. Koshelets, A. B. Ermakov, L. V. Filippenko, A. M. Baryshev, W. Luinge, J.-R. Gao, "Superconducting chip receivers for imaging application", *IEEE Trans. on Appl. Supercond.,* vol. 9**,** pp. 3773-3776, 1999.

[4] V. P. Koshelets, S. V. Shitov, "Integrated Superconducting Receivers", *Superconductor Science and Technology,* vol. 13, 2000, pp. R53-R69.

[5] S. V. Shitov, V. P. Koshelets, G. V. Prokopenko, L. V. Filippenko, A. B. Ermakov, "Superconducting integrated receiver as 400-600 GHz tester for coolable devices", to be presented at the *Conference on Applied Superconductivity*, Virginia Beach, USA, 17-23 Sept. 2000, report 4EA08.

[6] http://www.tuc.nrao.edu/mma/sites/

[7] S. V. Shitov, "Superconducting integrated receiver: design principle and numerical analysis", to be presented at the *Conference on Applied Superconductivity*, Virginia Beach, USA, 17-23 Sept. 2000, report 4EA07.

[8] S. Morohashi, and S. Hasuo, "Experimental investigations and analysis for high-quality Nb/Al-AlOx/Nb Josephson junctions", *J. Appl. Phis.,* vol. 61, pp. 4835-4849, 1987.

[9] T. Imamura, T. Shiota, and S. Hasuo, "Fabrication of high quality Nb/ AlOx-Al/Nb Josephson junctions: I – Sputtered Nb films for Junction electrodes", *IEEE Trans. on Appl. Supercond.,* vol. 2, pp. 1-14, 1992.

[10] M. Aoyagi, A. Shoji, S. Kosaka, F. Shinoki, and H. Hayakawa, "A 1 μm cross line junction process", in *Advances in Cryogenic Engineering Materials*, vol. 32, New York: Plenum, 1986, pp.557-563.

[11] M. Aoyagi, M. Maezawa, H. Nakagawa, I. Kurosawa, S. Takada, "An improved etching process used for the fabrication of submicron Nb/AlOx/Nb Josephson junctions", *IEEE Trans. on Appl. Supercond*., No 3, 1995.

[12] S. V. Shitov, V. P. Koshelets, S. A. Kovtonyuk, An. B. Ermakov, N. D. Whyborn and C.-O. Lindstrom, "Ultra-low-noise 100 GHz receiver based on parallel biased SIS arrays", *Supercond. Sci. Technol.,* vol. 4, pp. 406-408, 1991.

[13] M. M. T. M. Dierichs, R. A. Panhuyzen, C. E. Honingh, M. J. de Boer, T. M. Klapwijk, "Submicron niobium junctions for submillimeter-wave mixers using optical lithography", *Appl. Phys. Lett*., vol. 62, pp. 774-776, 1993.

[14] A. B. Ermakov, V. P. Koshelets, S. V. Shitov, A. M. Baryshev, W. Luinge, "A data acquisition system for test and control of superconducting integrated receivers", to be presented at the *Conference on Applied Superconductivity*, Virginia Beach, USA, 17-23 Sept. 2000, report 4EA10.